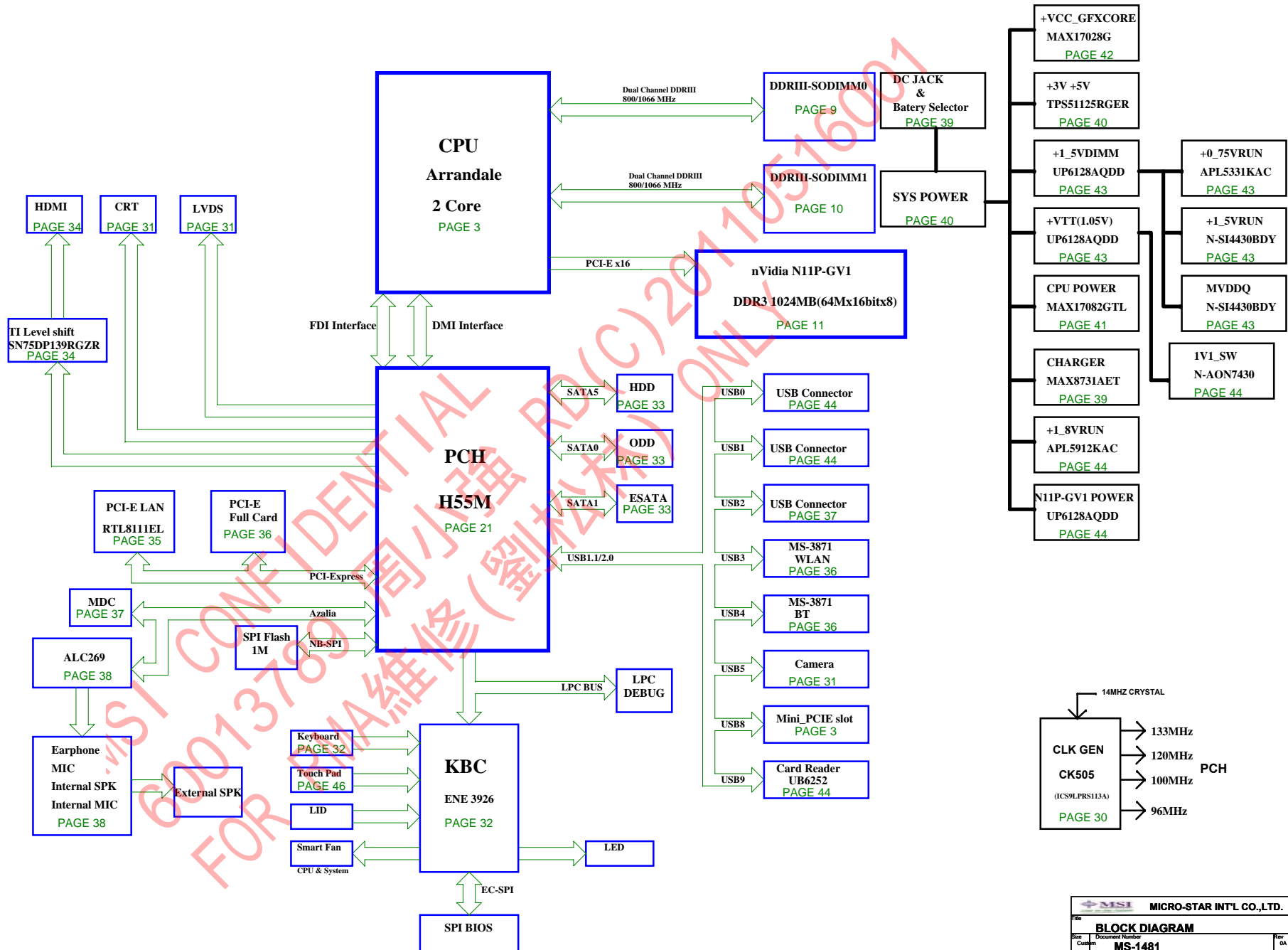


Table of Contents	
Page	Description
01 :	BLOCK DIAGRAM
02 :	PLATFORM
03 :	PROCESSOR-1 (HOST BUS)
04 :	PROCESSOR-2 (DDR3)
05 :	PROCESSOR-3 (POWER)
06 :	PROCESSOR-4 (GRAPHICS POWER)
07 :	PROCESSOR-5 (GND)
08 :	PROCESSOR-6 (RESERVE)
09 :	DDR3 SODIMM 0
10 :	DDR3 SODIMM 1
11 :	N11P-GV1 PCIE Host
12 :	N11P-GV1_MEM Interface A
13 :	N11P-GV1_MEM Interface C
14 :	N11P-GV1_FrameA DDR3 I
15 :	N11P-GV1_FrameA DDR3 II
16 :	N11P-GV1_FrameC DDR3 I
17 :	N11P-GV1_FrameC DDR3 II
18 :	N11P-GE1_Display Interface
19 :	N11P-GE1_Thermal, GPIOs
20 :	N11P-GE1 Power & GND
21 :	PCH-1 (HDA,JTAG,SATA)
22 :	PCH-2 (PCI-E,SMBUS,CLK)
23 :	PCH-3 (DMI,FDI,GPIO)
24 :	PCH-4 (LVDS,DDI)
25 :	PCH-5 (PCI,USB,NVRAM)
26 :	PCH-6 (GPIO,VSS_NCTF,RSVD)
27 :	PCH-7 (POWER)
28 :	PCH-8 (POWER)
29 :	PCH-9 (GND)
30 :	CLOCK GEN (ICS9LPRS113A)
31 :	CRT, LVDS,Camera
32 :	KBC/EC/uP (KB3926)
33 :	ODD,HDD,ESATA,LED,FAN
34 :	HDMI & SWITCH
35 :	GIGA LAN (RTL 8111EL)
36 :	WLAN,BT,Combo ,3G SIM CARD
37 :	MDC,USB
38 :	Audio ALC269
39 :	M_Battery select & Charger
40 :	M_System Power
41 :	M_CPU power
42 :	M_Graphic Core
43 :	M_SMDDR_VTERM /1_5VRUN
44 :	M_VTT Power,+1.8VRUN, NVVDD
45 :	1481A_Card Reader,Audio,USB
46 :	1481B_Lauch Board
47 :	1481C_T/P Board
48 :	Screw / ME
49 :	EMI
50 :	Power On Sequency
51 :	Power Down Sequency
52 :	Power MAP



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

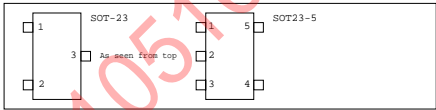
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
N11P_VDD_CORE	0.95V	S0	GPU core power
MVDDQ	1.5V	S0	GPU DDR3 power
1V1_SW	1.0V	S0	GPU PCIE power
+3VRUN_N11P	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

Suffix
V = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



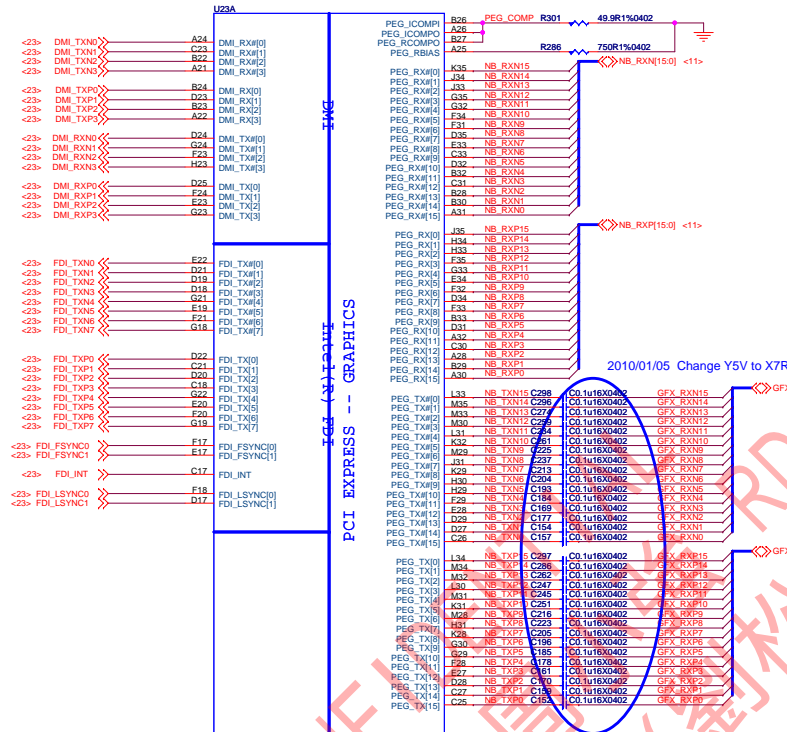
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



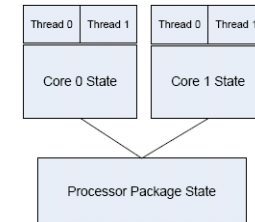
PGA988
IC_AUB_CFD_PGA_R0P9 N12-9890030-L06

Westmere (formerly Nehalem-C) is the name given to the 32 nm die shrink of Nehalem.

Brand Name	Model (list)	L3 Cache size	Thermal Design Power
Intel Core i3	i3-3xxM	3 MB	35 W
Intel Core i5	i5-4xxM	3 MB	35 W
	i5-5xxM	3 MB	35 W
Intel Core i7	i7-6xxUM	4 MB	18 W
	i7-6xxLM	4 MB	25 W
	i7-6xxM	4 MB	35 W

The Core i3-3xx will be similar to the Core i5-4xx series but running at lower clock speeds and without Turbo Boost

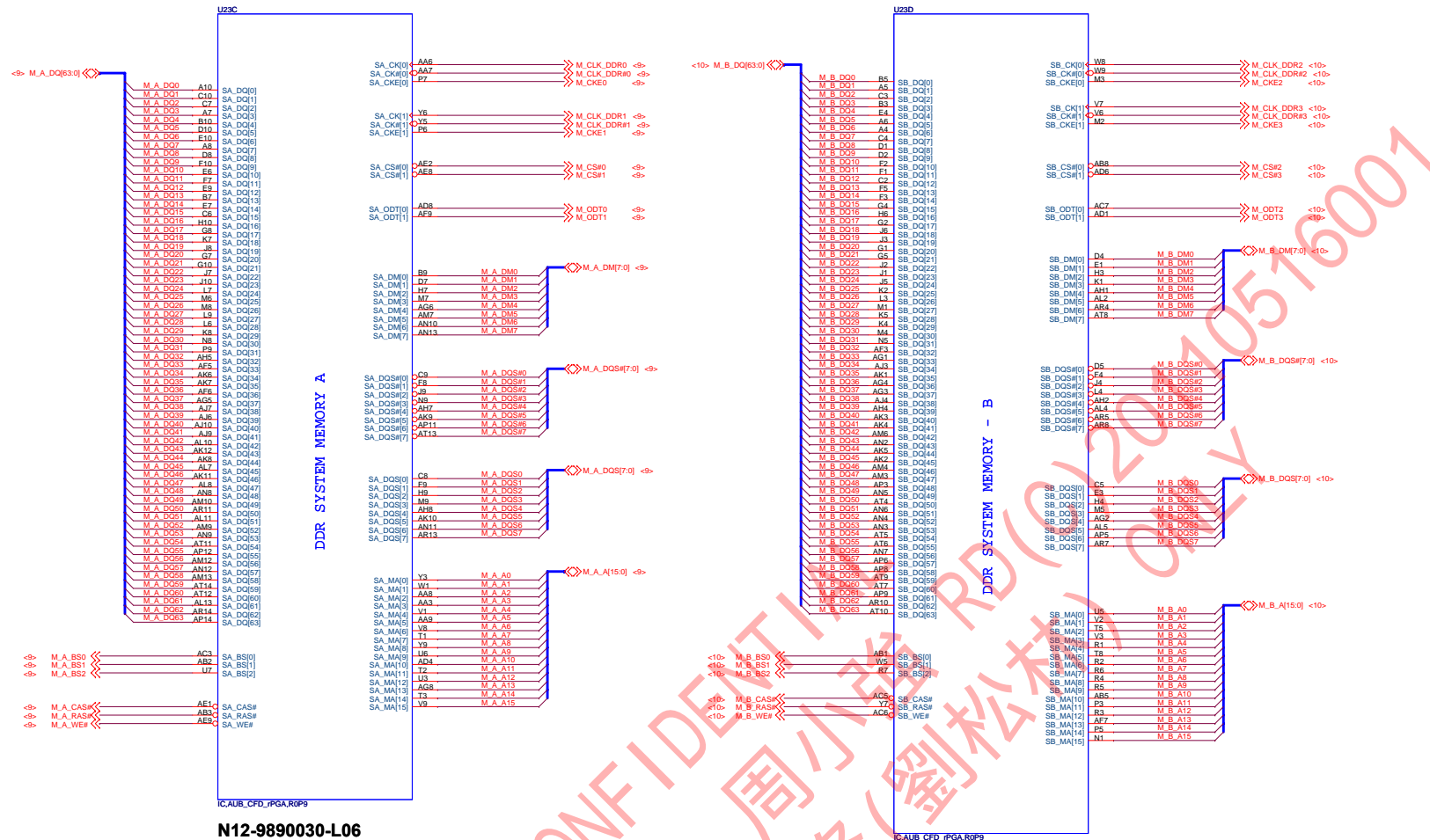
Brand	Intel Core i3	Intel Core i5	Intel Core i7	Intel Core i9	Intel Core i11	Intel Core i12	Intel Core i13
Segment	POP1	POP2	POP3	ULV1	ULV2	LV1	LV2
TDP	35W	35W	35W	18W	18W	25W	25W
Cores/ Threads	2/4	2/4	2/4	2/4	2/4	2/4	2/4
CPU Base Freq (GHz)	2.40	2.53	2.66	1.06	1.2	2.00	2.13
Intel® Turbo Boost Technology Max 9C Turbo (GHz)	2.93	3.06	3.33	2.13	2.26	2.80	2.93
DDR3 (MHz)	1066MHz	1066MHz	1066MHz	800MHz	800MHz	1066MHz	1066MHz
L3 Cache	3MB	3MB	4MB	4MB	4MB	4MB	4MB
Integrated Gfx	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gfx Base Render Frequency	500MHz	500MHz	500MHz	166MHz	166MHz	266MHz	266MHz
Intel® Turbo Boost Technology Max Gfx Render (MHz)	766MHz	766MHz	766MHz	500MHz	500MHz	566MHz	566MHz
Intel® Hyper-threading /VT/TXT/Intel® vPro	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	BGA/PGA	BGA/PGA	BGA/PGA	BGA	BGA	BGA	BGA



Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1			
Thread 0	C0	C0	C0	C3	C6
	C1	C0	C1 ¹	C1 ¹	C1 ¹
	C3	C0	C1 ¹	C3	C3
	C6	C0	C1 ¹	C3	C6

ARRANDALE PROCESSOR (DDR3)



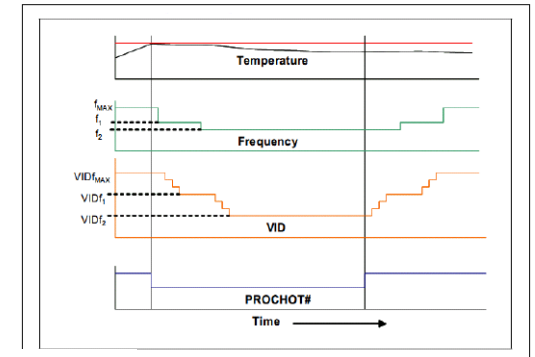
2010/01/12 remove external CLK from CLK GEN

Arrandale Reference Clocks

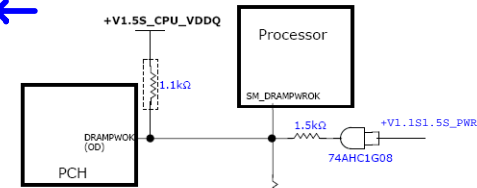
Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI/Intel® FDI
DPPLL_REF_SSCLK/DPPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort (eDP)

Signal Name	Description	Direction/Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input: The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROC_PWRGD output signal of the PCH.	I Asynchronous CMOS

Frequency and Voltage Ordering



N12-9890030-L06



SM_DRAMPWROK signal is driven low when PROCESSOR is turned off in S3 entry. During S3 exit, this signal is driven high only after +V1.5S_CPU_VDDQ stable. There is no timing requirement between and 0.75-V V_{TT} rail.

+V1.1S1.5S_PWRGD signal is an open-drain signal driven from +V1.5S_CPU_VDDQ PWRGOOD logic. It should go high only after +V1.5S_CPU_VDDQ to processor is stable.

DRAMPWROK behavior in S5/S4 to S0:

During S5/S4 to S0, DRAMPWROK is driven low by PCH until PCH_PWROK becomes high provided SLP_S4# is high. Even though DRAMPWROK derived from PWRGOOD of +V1.5S_CPU_VDDQ comparator, it is overdriven to low by PCH until PCH_PWROK goes high. This implementation ensures that S5 to S0 timings are maintained.

DRAMPWROK behavior in S0 to S3:

This signal is driven low as the +V1.1S1.5S_PWRGD becomes low when +V1.5S_CPU_VDDQ ramps down. To maintain this signal low, this AND gate is powered using SUS rail (+V3.3A). Any buffer/AND gate of 4 mA should work fine in the given circuit.

DRAMPWROK behavior in S3 to S0:

This signal is driven high when +V1.5S_CPU_VDDQ to the processor is stable

DRAMPWROK is 1.1-V/1.05-V signal to processor; hence a resistor divider is implemented to level translate the signal.

Refer to the latest Intel CRB schematics for more details on +V1.1S1.5S_PWRGD generation.

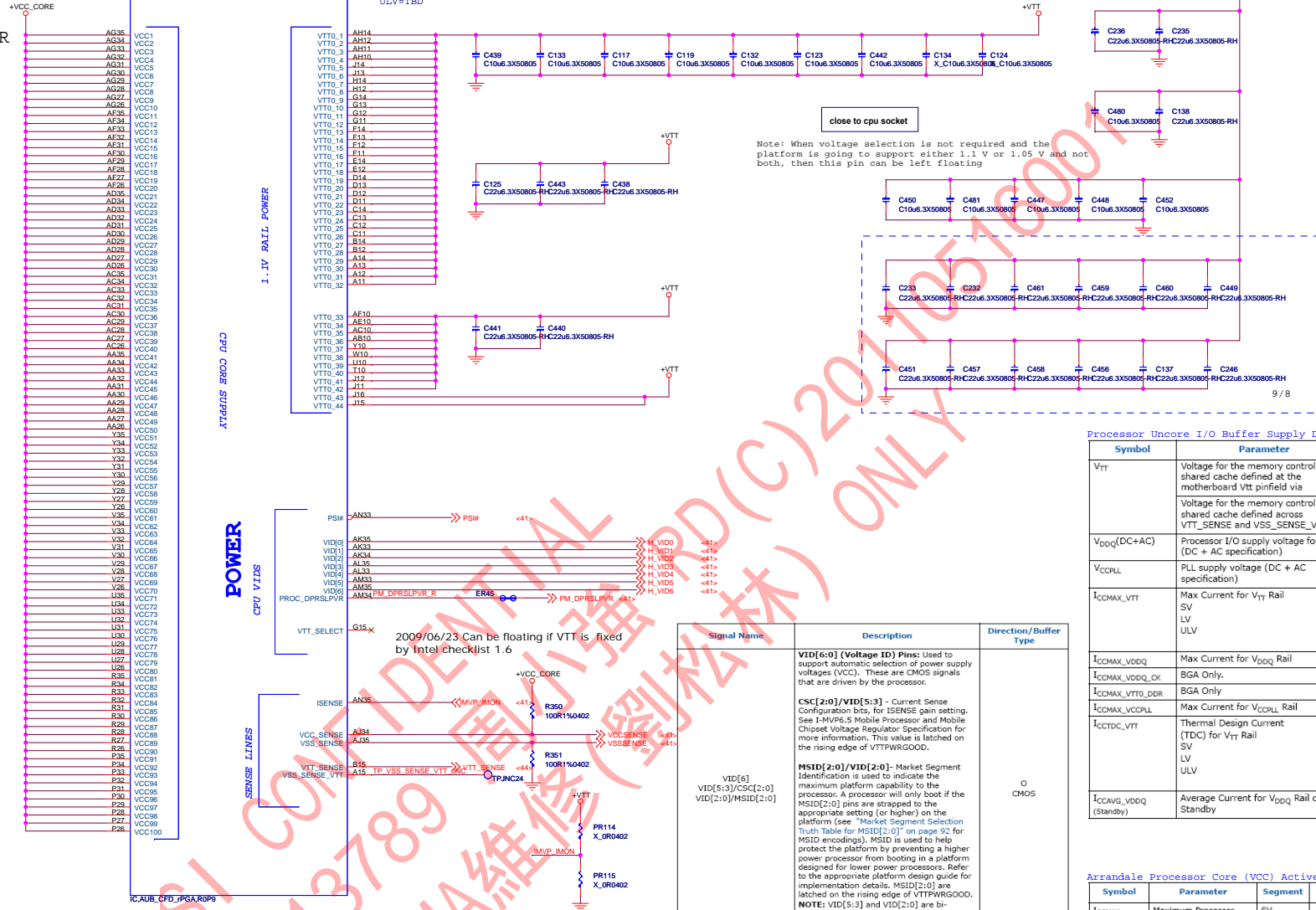
ARRANDALE PROCESSOR (POWER)

ARRANDALE:
SV=48A
LV=35A
ULV=27A

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER

PROCESSOR CORE POWER



Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V _{TT}	Voltage for the memory controller and shared cache defined at the motherboard VTT pinfield via VTT_SENSE and VSS_SENSE_VTT	0.9975	1.05	1.1025	V
V _{DDQ} (DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	0.9765	1.05	1.1235	V
V _{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V
I _{CCMAX_VTT}	Max Current for V _{TT} Rail SV LV ULV	-	-	18 16 16	A
I _{CCMAX_VDDQ}	Max Current for V _{DDQ} Rail	-	-	3	A
I _{CCMAX_VDDQ_OK}	BGA Only.	-	-	0.2	A
I _{CCMAX_VTT0_DDR}	BGA Only	-	-	2.6	A
I _{CCMAX_VCCPLL}	Max Current for V _{CCPLL} Rail	-	-	1.35	A
I _{CTDC_VTT}	Thermal Design Current (TDC) for V _{TT} Rail SV LV ULV	-	-	18 16 16	A
I _{CAVG_VDDQ}	Average Current for V _{DDQ} Rail during Standby	-	-	0.33	A

Arrandale Processor Core (VCC) Active and Idle Mode DC Voltage and Current

Symbol	Parameter	Segment	Min	Typ	Max	Unit
I _{CCMAX}	Maximum Processor Core I _{CC}	SV LV ULV	-	-	48 35 27	A
I _{CC_TDC}	Thermal Design I _{CC}	SV LV ULV	-	-	32 22 16	A
I _{CC_LFM}	I _{CC} at LFM	SV LV ULV	-	-	18 12 8	A
I _{CS}	I _{CC} at C6 Idle-state	SV LV ULV	-	-	0.3 0.3 0.3	A

N12-9890030-L06

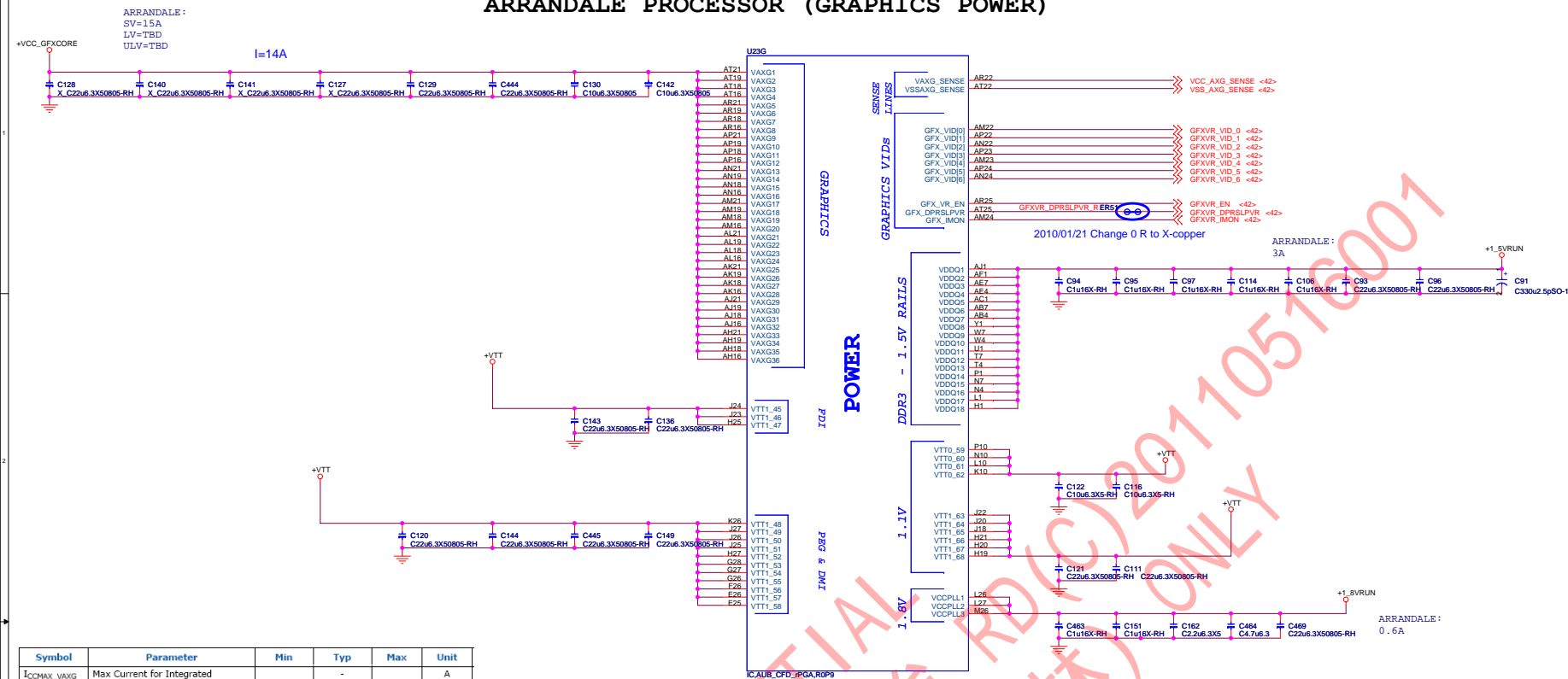
Table 17. IA Core I_{MAX} and Gain Definition - Defined Relative to CPU Core Maximum Current

CPU SKU, I _{CC_CORE-MAX} Maximum CPU Core Current	I _{MAX} (IMON=900 mV [A])	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
I _{CC_CORE-MAX} ≤ 20 A	20	001	45.0
20A < I _{CC_CORE-MAX} ≤ 30 A	30	010	30.0
30A < I _{CC_CORE-MAX} ≤ 40 A	40	011	22.5
40A < I _{CC_CORE-MAX} ≤ 50 A	50	100	18.0
50A < I _{CC_CORE-MAX} ≤ 60 A	60	101	15.0
60A < I _{CC_CORE-MAX} ≤ 70 A	70	110	12.9
70A < I _{CC_CORE-MAX} ≤ 90 A	90	111	10.0

Table 43. Market Segment Selection Truth Table for MSID[2:0]

MSID[2]	MSID[1]	MSID[0]	Description ^{1,2}
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Arrandale Standard Voltage (SV) 35W Supported
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

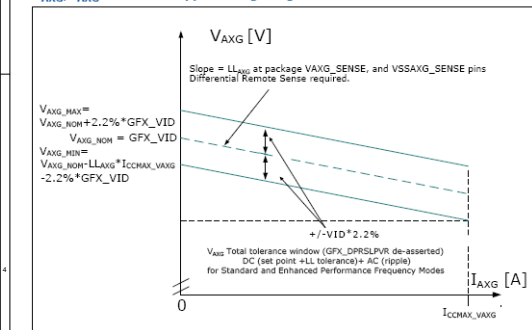
ARRANDALE PROCESSOR (GRAPHICS POWER)



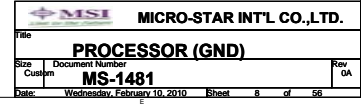
Symbol	Parameter	Min	Typ	Max	Unit
ICCHMAX_VA _{VG}	Max Current for Integrated Graphics Rail SV LV ULV			22 15 12	A
ICTDC_VA _{VG}	Thermal Design Current (TDC) for Integrated Graphics Rail SV LV ULV			12 7 6	A

Symbol	Parameter	Min	Typ	Max	Unit
V _{AXG}	Graphics core voltage		See Figure 15		

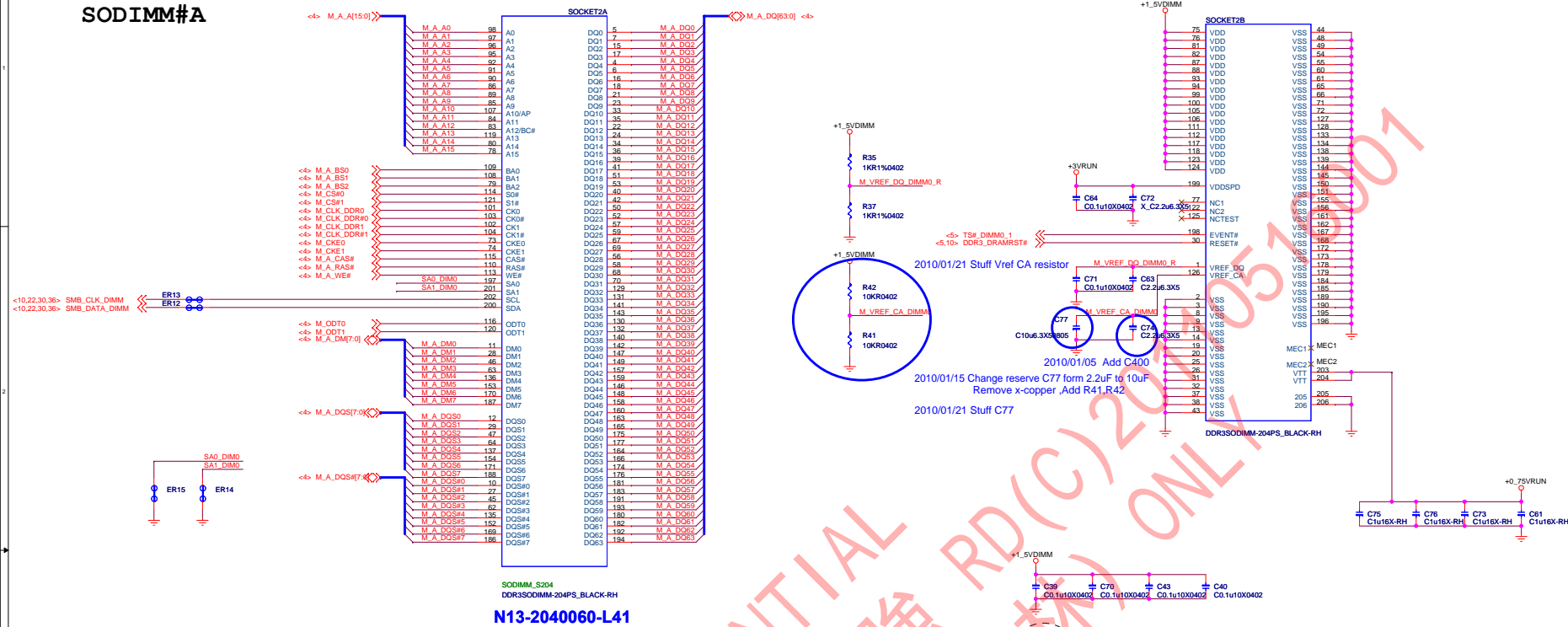
V_{AXG}/I_{AXG} Static and Ripple Voltage Regulation



ARRANDALE PROCESSOR (RESERVED)



SODIMM#A



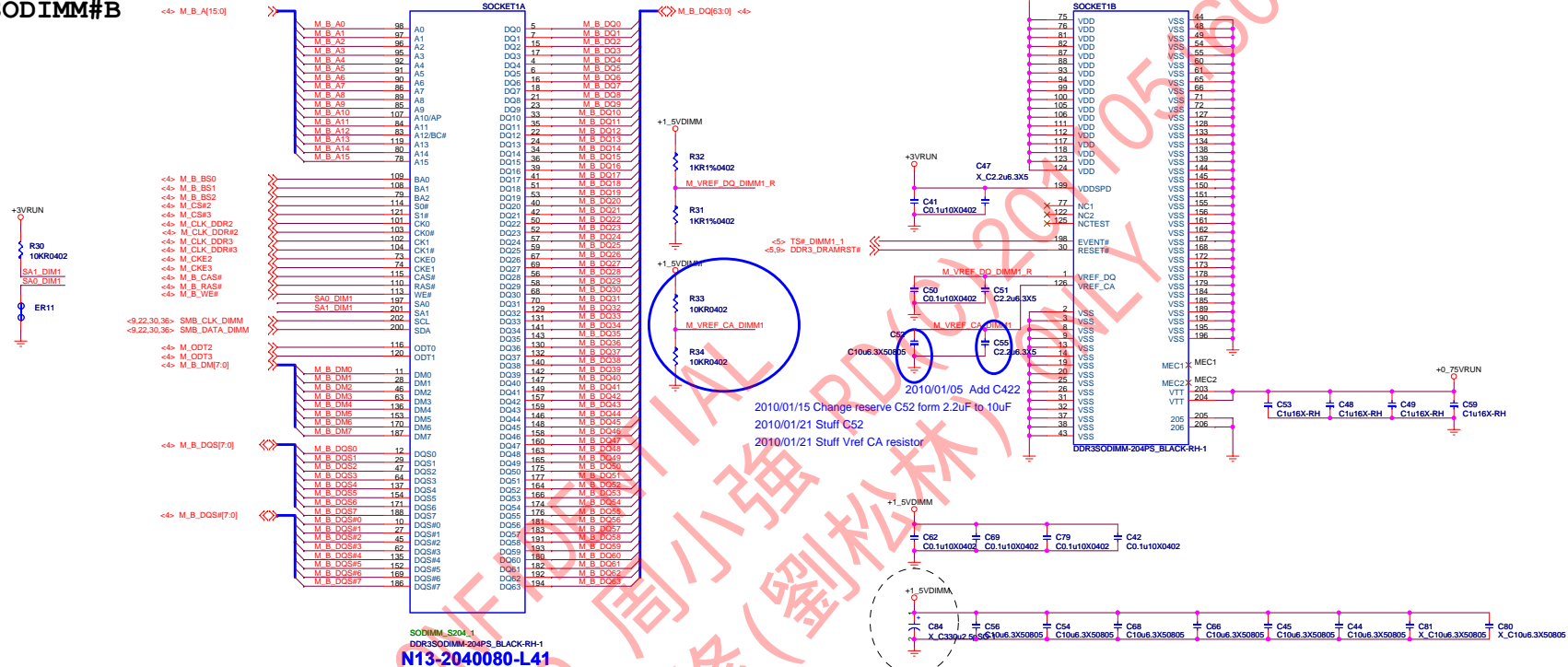
SODIMM_S204
DDR3SODIMM-204PS_BLACK-RH
N13-2040060-L41

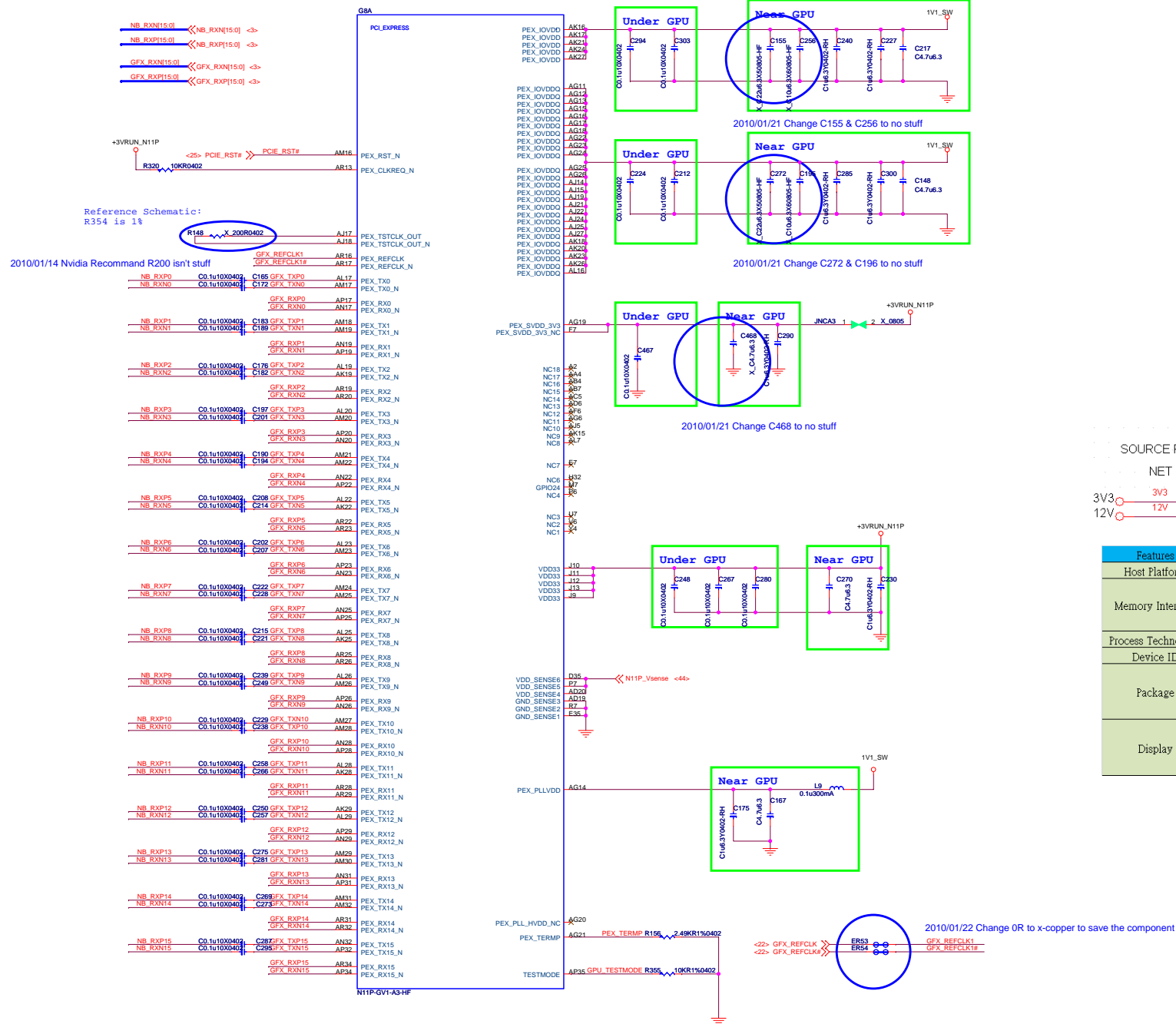
DDR3 SDRAM, 2GB, 667 (1333) MHz, TRANSCEID/TS256MSR64V3U

IDD Specification parameters Definition
(IDD values are for full operating range of voltage and Temperature)

Parameter	Symbol	Max.	Unit
Operating One bank Active-Precharge current: ICK = ICK(IDD), IRAS = IRAS(IDD), CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING.	IDD0	1.200	mA
Operating One bank Active-read-Precharge current: IOU = 0mA, BL = 8, CL = CL(IDD), AL = 0, ICK = ICK(IDD), IRAS = IRAS(IDD), IRCD = IRCD(IDD), CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1	1.300	mA
Precharge power-down current: All banks idle; ICK = ICK(IDD), CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2P	800	mA
Precharge quiet standby current: All banks idle; ICK = ICK(IDD), CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2Q	900	mA
Precharge standby current: All banks idle; ICK = ICK(IDD), CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N	900	mA
Active power-down current: All banks open; ICK = ICK(IDD), CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P	800	mA
Active standby current: All banks open; ICK = ICK(IDD), IRAS = IRAS(IDD), RP = RP(IDD), CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	1.000	mA
Operating burst read current: All banks open; Continuous burst reads; IOU = 0mA, BL = 8, CL = CL(IDD), AL = 0, ICK = ICK(IDD), IRAS = IRAS(IDD), RP = RP(IDD), CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R	2.120	mA
Operating burst write current: All banks open; Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0, ICK = ICK(IDD), IRAS = IRAS(IDD), RP = RP(IDD), CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W	2.320	mA
Burst refresh current: ICK = ICK(IDD); Refresh command at every tREF(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	2.240	mA
Self refresh current: CK and /CK at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6	100	mA
Operating bank interleave read current: All bank interleaving reads; IOU = 0mA, BL = 8, CL = CL(IDD), AL = 0, ICK = ICK(IDD), IRAS = IRAS(IDD), RP = RP(IDD), IRCD = IRCD(IDD), CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during Despects; Data pattern is same as IDD4R.	IDD7	3.400	

SODIMM#B





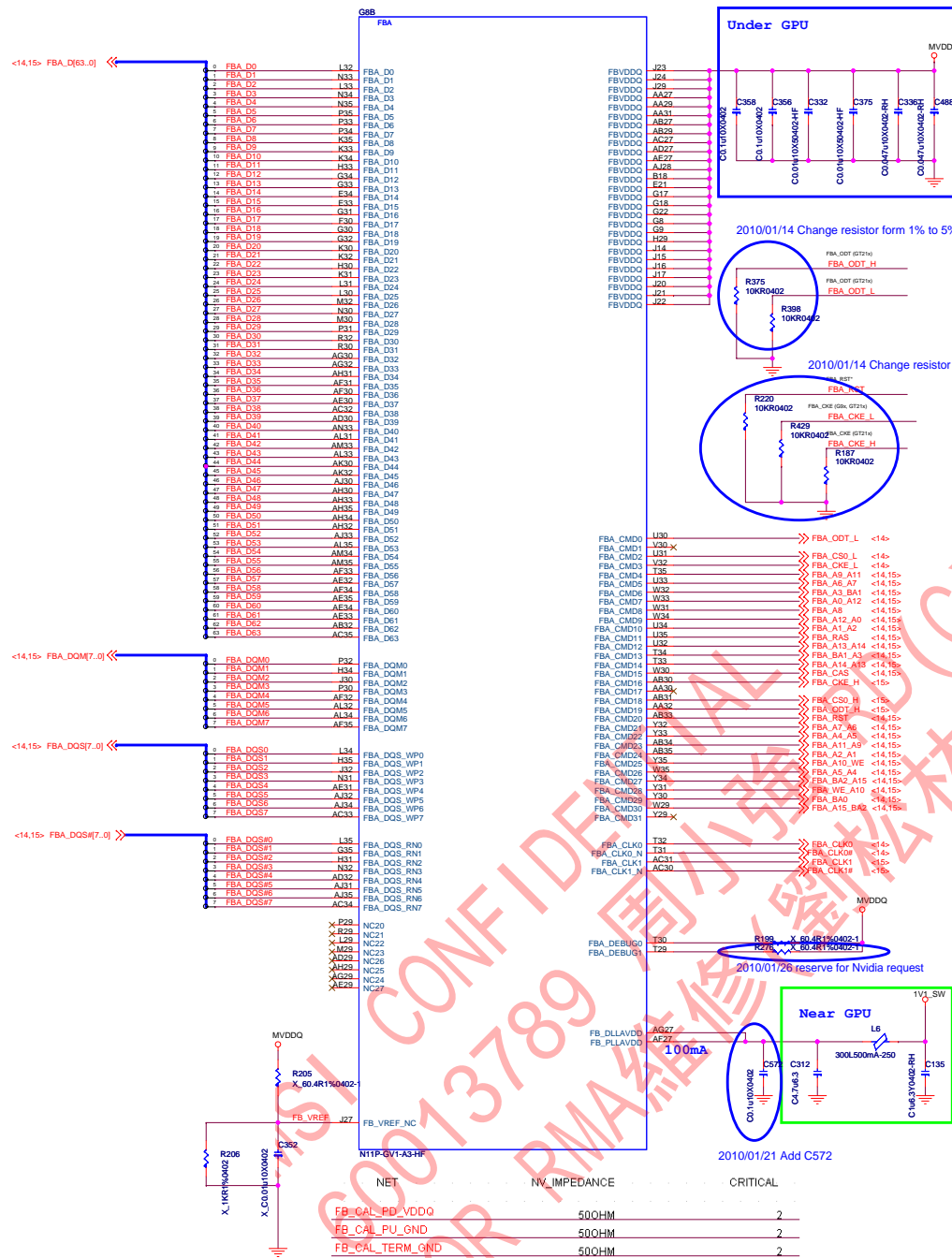
Optimus Software Design for Arrandale Platforms

At POST, the system BIOS should initialize the IGP as the primary graphics adapter. As the OS initializes, both the IGP driver and GPU driver will load. Up to this point the platform is similar to any multiple graphics adapter system-such as a desktop system with more than one graphics card installed. However, the GPU in an Optimus system typically has no physical display outputs. It is purely a graphics rendering and compute device. Then Optimus software will determine when the GPU's capabilities are needed and will enable the GPU as needed, and will host work for individual applications on the GPU as needed.

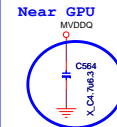
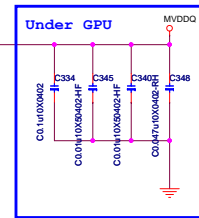
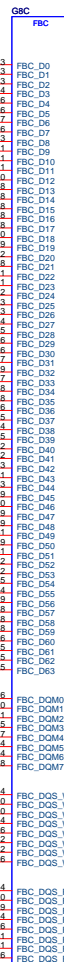
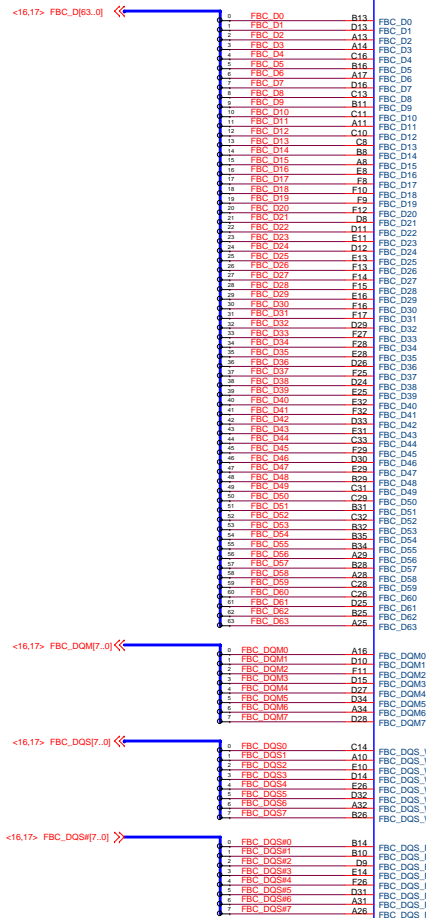
DIFFPAIR	IMPEDANCE	CRITICAL
PEX_TX	90DIFF	1
PEX_TX	90DIFF	1
DIFFPAIR	IMPEDANCE	CRITICAL
PEX_RX	90DIFF	1
PEX_RX	90DIFF	1
DIFFPAIR	IMPEDANCE	CRITICAL
PEX_CLK_OUT	90DIFF	1
PEX_CLK_OUT	90DIFF	1

NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE	POWER_NET
3V3	3V3	16.00	4A	3.30000V
12V	12V	25.00	8A	18.0000V

Features	N11P-GE1	N11P-LP1	N11P-GS1
Host Platform	PCIe 2.0 x 16		
Memory Interface	128-bit DDR3 GDDR3		128-bit DDR3 GDDR3 GDDR5
Process Technology	40nm		
Device ID	0x0A29	0x0A2B	0x0CAF
Package	969-ball BGA 29nm x 29nm package BG1-128		
Display	DVII DVID 1920 x 1200 @ 60Hz	DVII DVID 2560 x 1600 @ 60Hz	

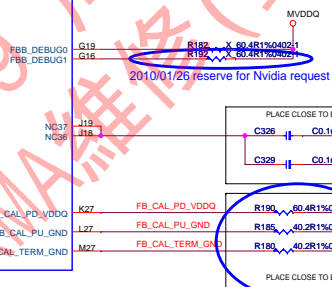


GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
Fb_C00	Fb_C00	CKE	CKE
Fb_C01	Fb_C08	A8	A8
Fb_C02	Fb_C02	C6P	
Fb_C03	Fb_C021	A7	A6
Fb_C04	Fb_C04	A2	A1
Fb_C05	Fb_C023	A11	A9
Fb_C06	Fb_C026	A5	A4
Fb_C07	Fb_C07	A0	A15
Fb_C08	Fb_C015	CAS*	CAS*
Fb_C09	Fb_C013	BA1	A3
Fb_C010	Fb_C04	A9	A11
Fb_C011	Fb_C018		C5P*
Fb_C012	Fb_C029	BA0	BA0
Fb_C013	Fb_C027	BA2	A15
Fb_C014	Fb_C06	A3	BA1
Fb_C015	Fb_C017		C51*
Fb_C016	Fb_C019		ODT
Fb_C017	Fb_C022	A4	A5
Fb_C018	Fb_C012	A13	A14
Fb_C019	Fb_C028	WE*	A10
Fb_C020	Fb_C010	A1	A2
Fb_C021	Fb_C025	A10	WE*
Fb_C022	Fb_C09	A12	A0
Fb_C023	Fb_C01	C51*	
Fb_C024	Fb_C011	RA5*	RA5*
Fb_C025	Fb_C00	ODT	
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
Fb_C026	Fb_C05	A6	A7
Fb_C027	Fb_C016	CKE	
Fb_C028	Fb_C020	R5T	R5T
Fb_C029	Fb_C014	A14	A13
Fb_C030	Fb_C030	A15	BA2
Not Available	Fb_C031		



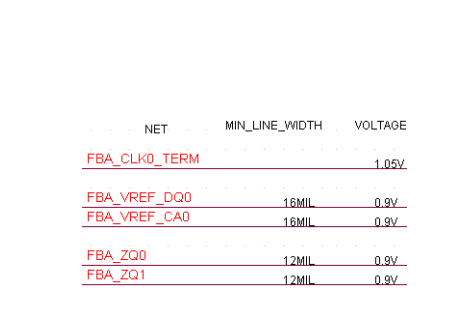
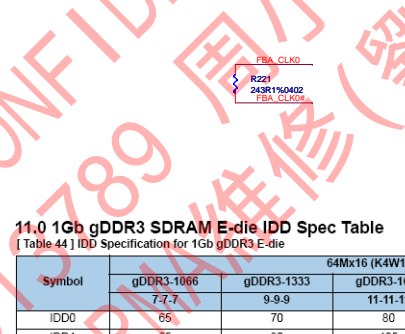
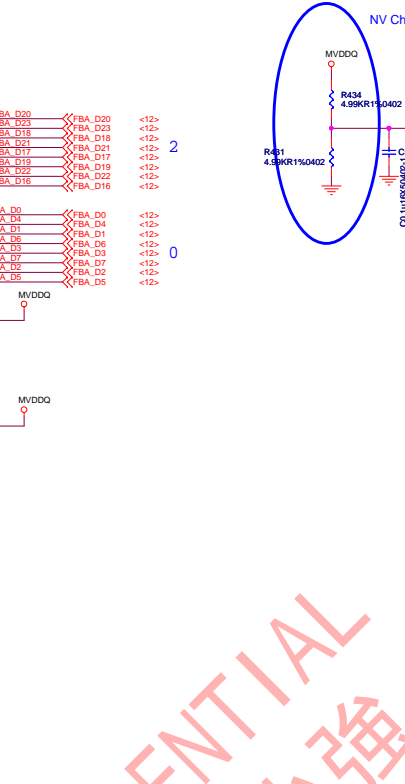
2010/01/21 Change C564 to no stuff

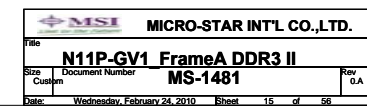
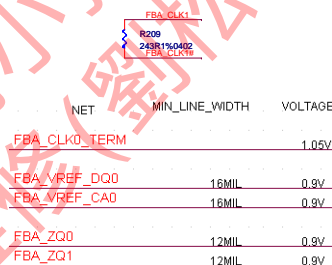
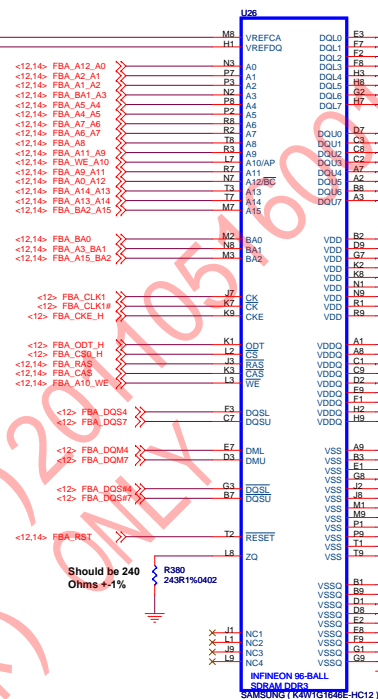
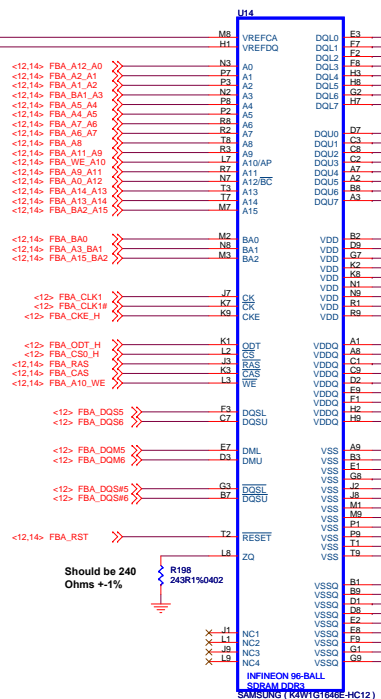
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FbX_CMD0	FbX_CMD3	CKE	
FbX_CMD1	FbX_CMD8	A8	A8
FbX_CMD2	FbX_CMD21	CAP	
FbX_CMD3	FbX_CMD24	A7	A6
FbX_CMD4	FbX_CMD27	A2	A1
FbX_CMD5	FbX_CMD30	A11	A9
FbX_CMD6	FbX_CMD33	A5	A4
FbX_CMD7	FbX_CMD36	A0	A15
FbX_CMD8	FbX_CMD39	CAS*	CAS*
FbX_CMD9	FbX_CMD42	BA1	A3
FbX_CMD10	FbX_CMD45	A9	A11
FbX_CMD11	FbX_CMD48	C0*	
FbX_CMD12	FbX_CMD51	BA0	BA0
FbX_CMD13	FbX_CMD54	BA2	A15
FbX_CMD14	FbX_CMD57	A3	BA1
FbX_CMD15	FbX_CMD60	C51*	
FbX_CMD16	FbX_CMD63		ODT
FbX_CMD17	FbX_CMD66	A4	A5
FbX_CMD18	FbX_CMD69	A13	A14
FbX_CMD19	FbX_CMD72	WE*	A10
FbX_CMD20	FbX_CMD75	A1	A2
FbX_CMD21	FbX_CMD78	A10	WE*
FbX_CMD22	FbX_CMD81	A12	A0
FbX_CMD23	FbX_CMD84	C51*	
FbX_CMD24	FbX_CMD87	RA5*	RA5*
FbX_CMD25	FbX_CMD90	ODT	
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FbX_CMD26	FbX_CMD93	A6	A7
FbX_CMD27	FbX_CMD96		
FbX_CMD28	FbX_CMD99	RST	RST
FbX_CMD29	FbX_CMD102	A14	A13
FbX_CMD30	FbX_CMD105	A15	BA2
Not Available	FbX_CMD108		



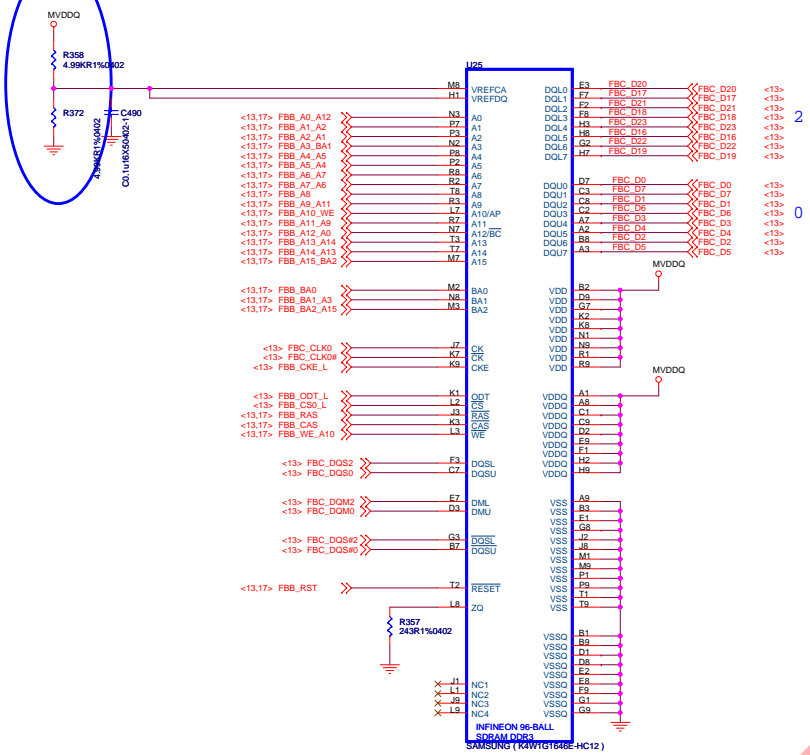
NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

NV Check those value is correct

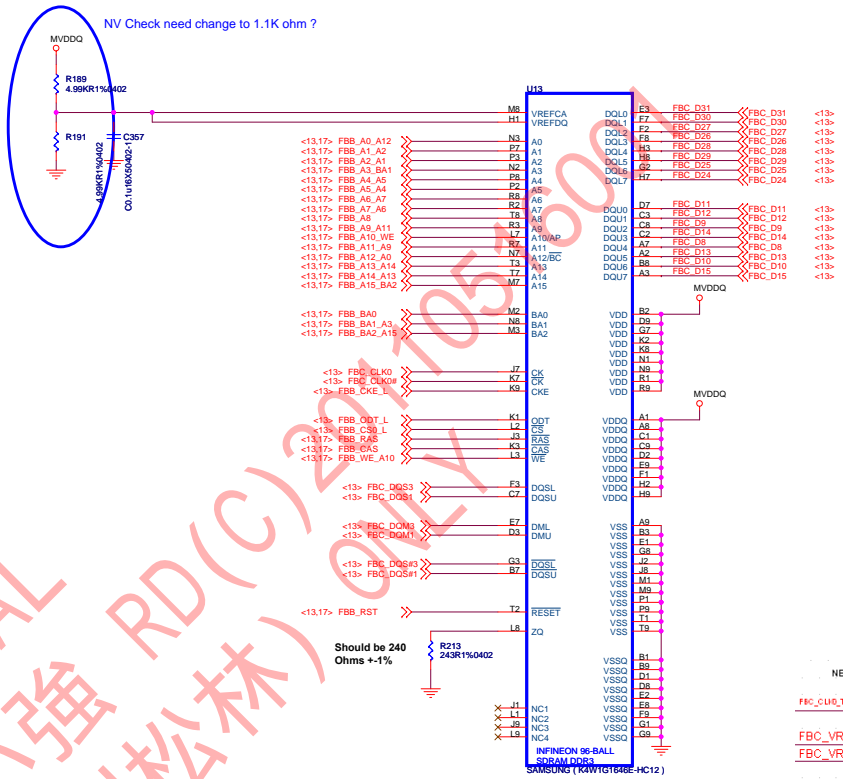




NV Check need change to 1.1K ohm ?

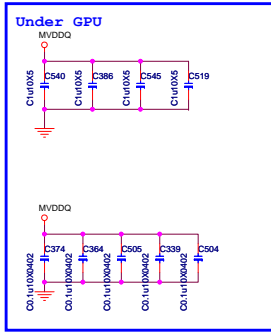
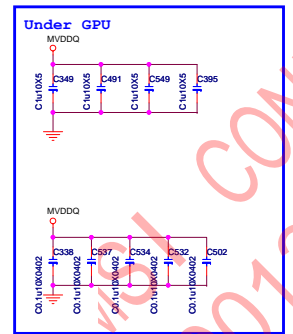


NV Check need change to 1.1K ohm ?

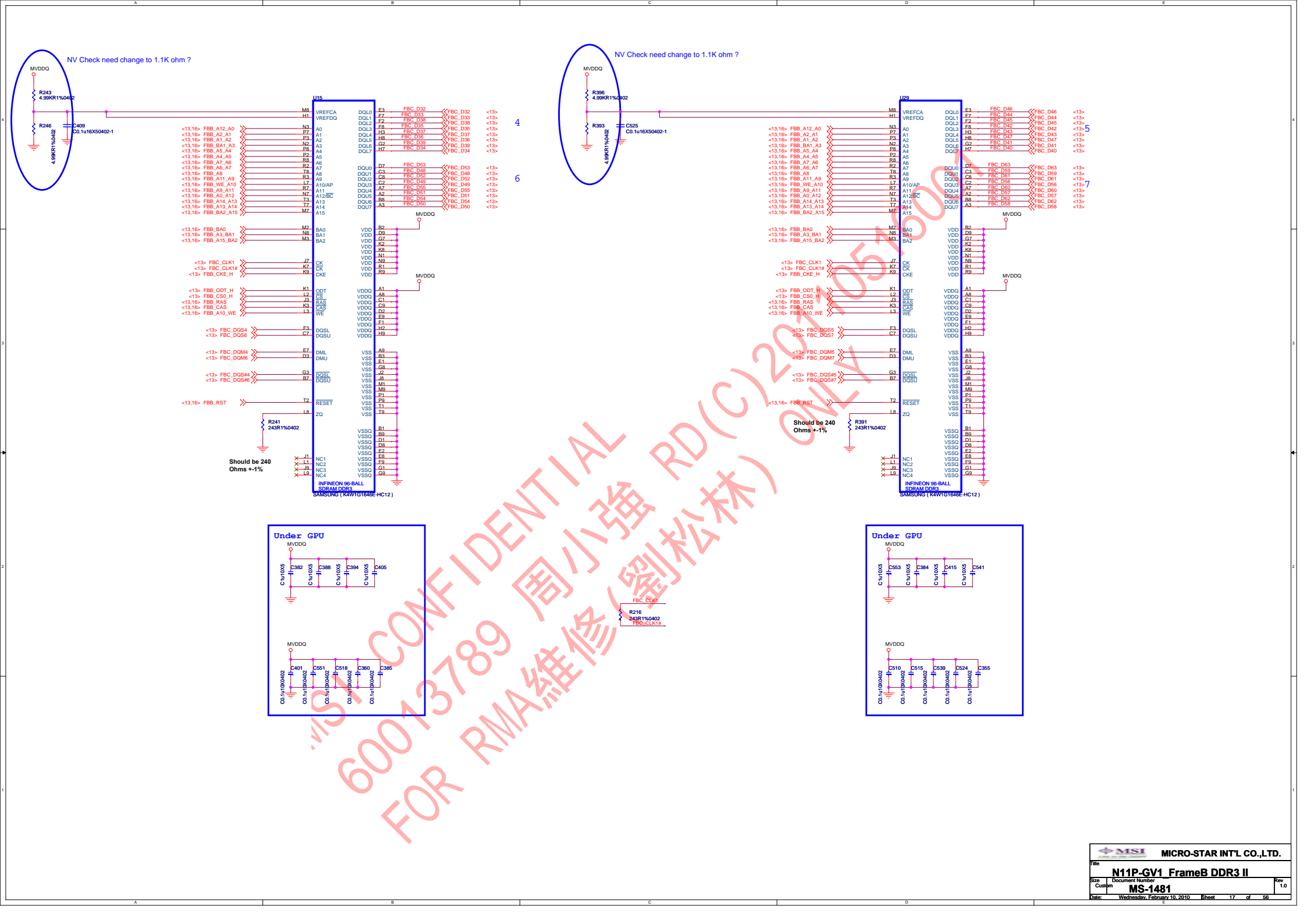


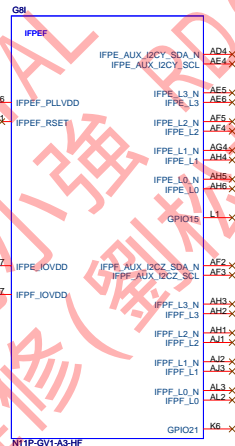
Should be 240 Ohms +/-1%

R213 243R1%0402



NET	MIN_LINE_WIDTH	VOLTAGE
FBC_CLK0_TERRM		1.05V
FBC_VREF_DQ0	16MIL	0.9V
FBC_VREF_CA0	16MIL	0.9V
FBC_Z00	12MIL	0.9V
FBC_Zq1	12MIL	0.9V






Title		MICRO-STAR INT'L CO.,LTD	
Size		N11P-GV1 Display Interface	
Customer		Document Number MS-1481	



Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_S0	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVCFG[4]	SUB_VENDER	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_S1	VDD33	RAMCFG0[3]	RAMCFG0[2]	RAMCFG0[1]	RAMCFG0[0]



 MICRO-STAR INT'L CO.,LTD.	
Title N11P-GV1 Thermal, GPIOs	
Size Custom	Document Number MS-1481
Date: Wednesday, February 10, 2010	Sheet 19 of 56

DA-04881-001_V04
DA-04882-001

Products	GPU (W)	Mem (W)	NVCLK/MCLK (MHz)
N11P-G01 1024MB DDR3	22.96	5.07	575/790
N11P-LP1 1024MB DDR3	14.81	4.78	475/700
N11P-G01 1024MB DDR3	22.85	4.97	450/790

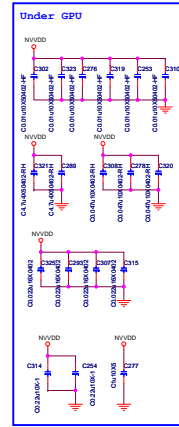
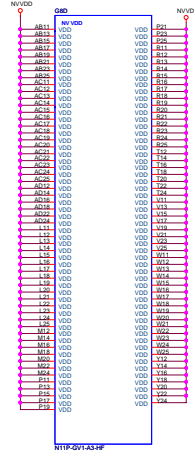
Products	NVYDD
N11P-G01 1024MB DDR3	0.95V 21.4A 20.33W
N11P-LP1 1024MB DDR3	0.85V 14.37A 12.22W
N11P-G01 1024MB DDR3	0.9V 22.19A 19.97W

Products	FBVDD 1.5V		FBVDDQ GPU+Mem 1.5V	
N11P-G01 1024MB DDR3	1.84A	2.76W	2.56A	3.84W
N11P-LP1 1024MB DDR3	1.69A	2.54W	2.48A	3.73W
N11P-G01 1024MB DDR3	1.52A	2.28W	2.98A	4.48W

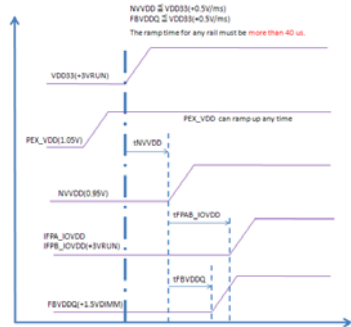
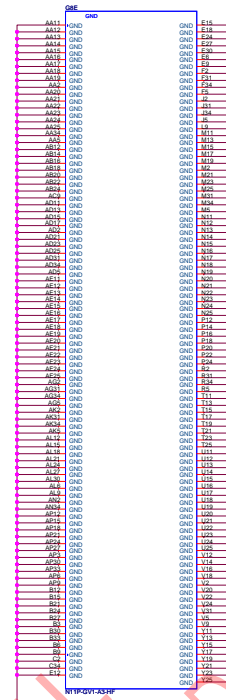
Products	PCI Express 1.05V	IO PLLVDD 1.05V
N11P-G01 1024MB DDR3	599.27mA 0.63W	186.77mA 0.2W
N11P-LP1 1024MB DDR3	581.74mA 0.61W	186.77mA 0.2W
N11P-G01 1024MB DDR3	578mA 0.61W	186mA 0.2W

Products	IO PLLVDD 1.8V
N11P-G01 1024MB DDR3	88.5mA 0.16W
N11P-LP1 1024MB DDR3	88.5mA 0.16W
N11P-G01 1024MB DDR3	87mA 0.16W

Products	Other 3.3V
N11P-G01 1024MB DDR3	39.97mA 0.13W
N11P-LP1 1024MB DDR3	39.97mA 0.13W
N11P-G01 1024MB DDR3	39mA 0.13W

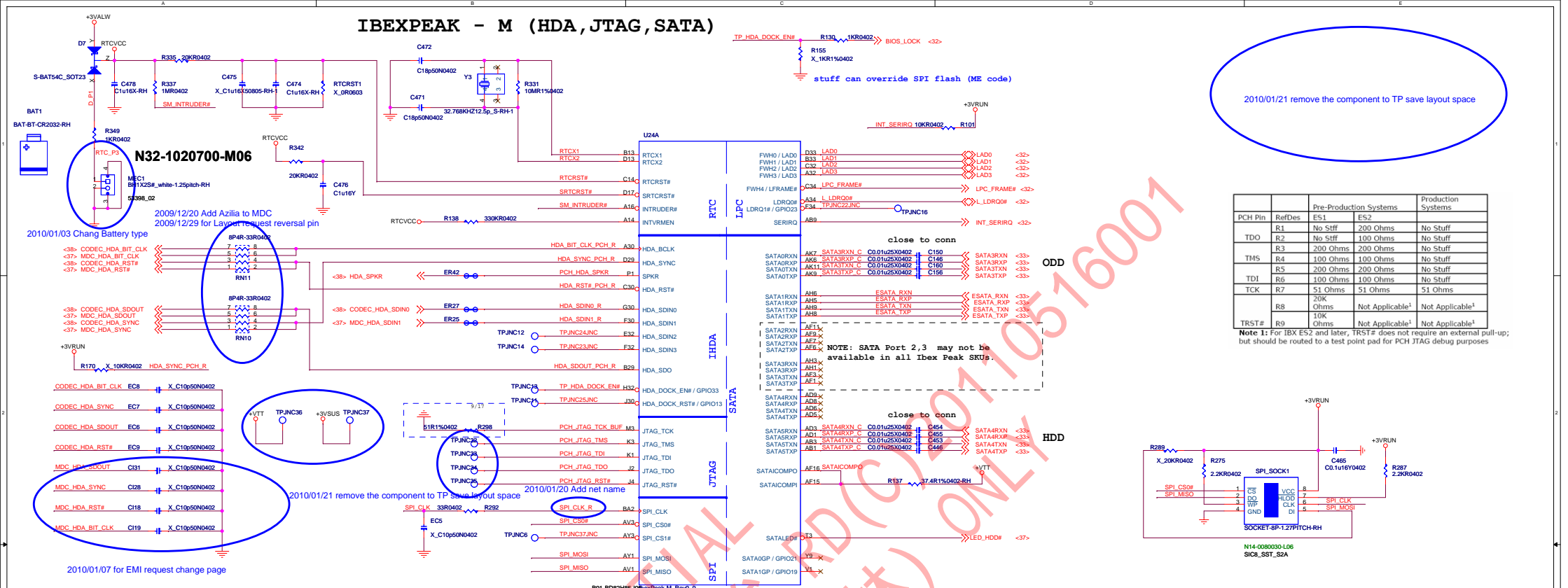


Near GPU



CONFIDENTIAL 周小強 (劉松林) ONLY

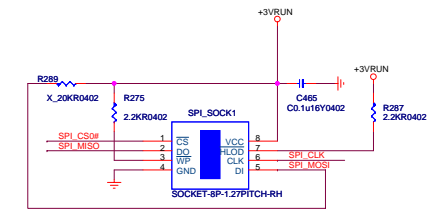
IBEXPEAK - M (HDA, JTAG, SATA)



2010/01/21 remove the component to TP save layout space

PCH Pin	RefDes	Pre-Production Systems	Production Systems
TDO	R1	No Stiff	200 Ohms
	R2	No Stiff	100 Ohms
	R3	200 Ohms	200 Ohms
TMS	R4	100 Ohms	100 Ohms
	R5	200 Ohms	200 Ohms
TDI	R6	100 Ohms	100 Ohms
TCK	R7	51 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable ¹
TRST#	R9	10K Ohms	Not Applicable ¹

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes



N14-0080030-L06
SIC8_SST_S2A



2101/01/25 BIOSPN pending change to M31-25L3203-M24

SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor
Disable iTPM: Left floating, no pull-down required.

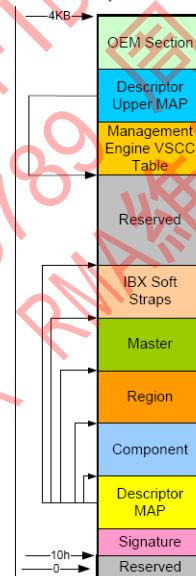
Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, the assertion of MEPWROK or deassertion of LAN_RST#. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPI_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ibex Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

Flash Descriptor

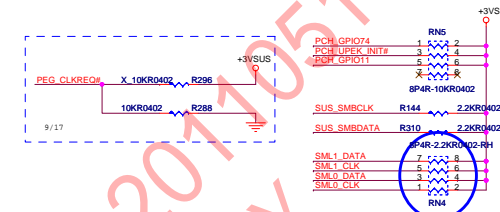
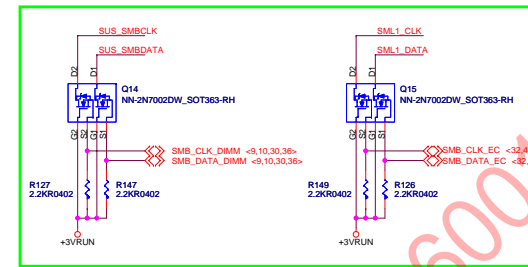
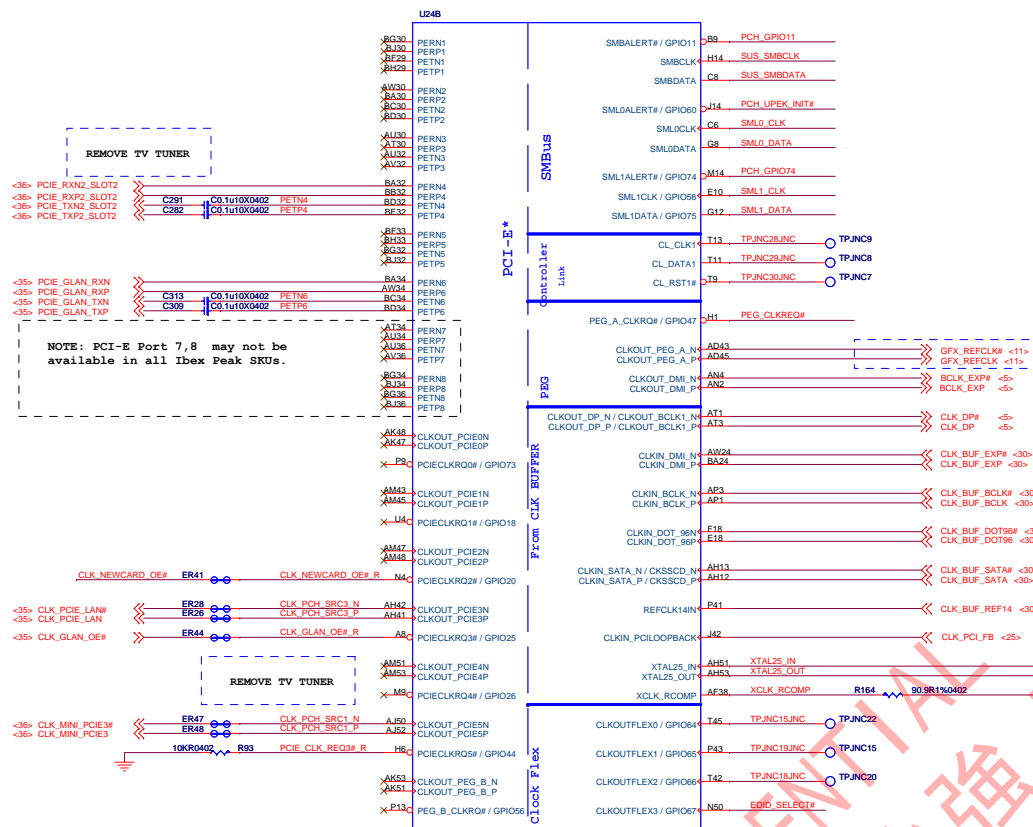


- The Flash signature at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is NOT used by Intel® ME Ignition FW only. BIOS and GbE write and erase capabilities depend on LVSCC and UVSCC registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

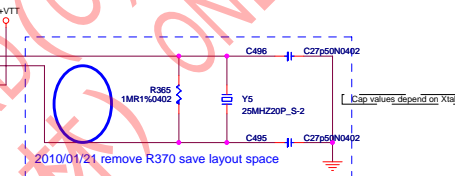
Region Access Control Table

Master Read/Write Access			
Region	CPU and BIOS	ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

IBEXPEAK - M (PCI-E, SMBUS, CLK)



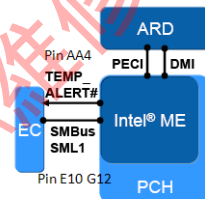
2009/12/29 RN8 reversal for layout request



2010/01/21 remove R370 save layout space

PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKREQ# PEG_B_CLKREQ#	SUS Well

1. Processor turbo – Most challenging in terms of power density, drives Heat Exchanger design
2. GFX turbo – Doesn't affect Heat Exchanger design, just ensures that Thermal Interface Material is capable
3. TDP (Legacy) – Slightly relaxed Heat Exchanger design



- Turbo Boost control– EC passes parameters through PCH to host software for real-time Turbo Boost control.
- PCH can be programmed to notify EC when a device is outside of limits via TEMP_ALERT# signal– No SW alert in PCH.

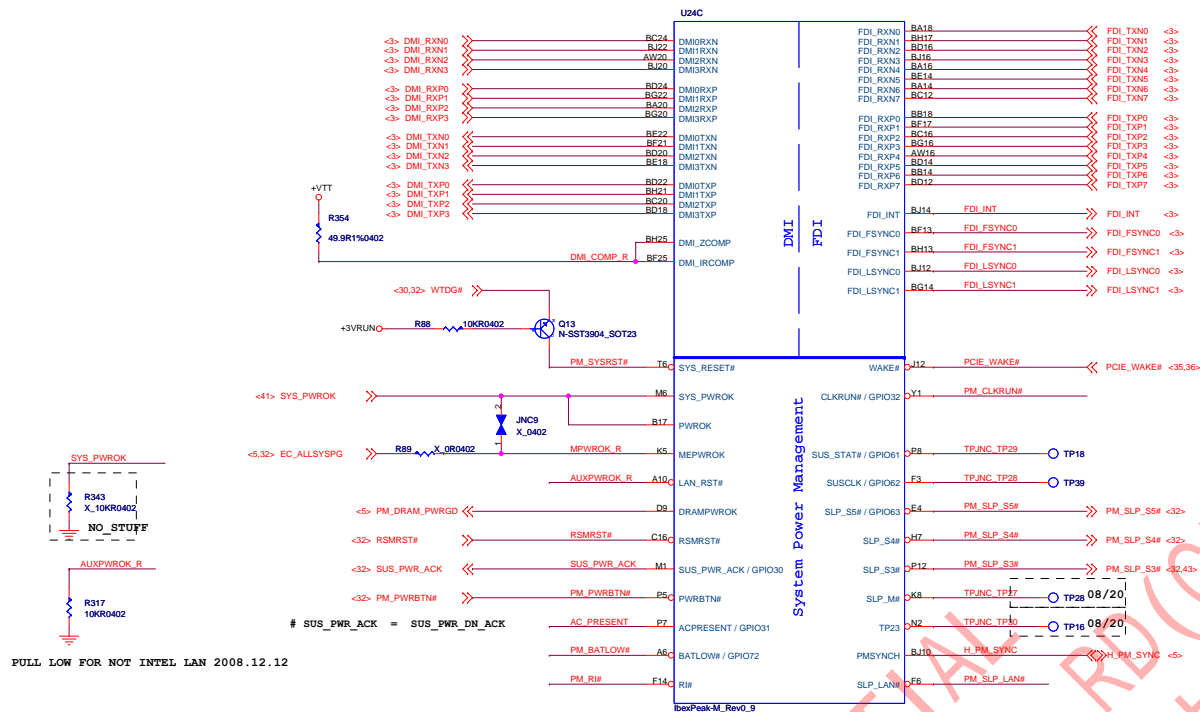
- EC can read from PCH via SMBus:
 - Temperatures
 - CPU, GMCH
 - Sequence number
 - Host status
- EC can write to PCH via SMBus:
 - Disable and enable power sharing
 - CPU and package power clamps
 - Biasing preference
 - Upper and lower temperature limits
 - CPU, MCH
 - TEMP_ALERT# trip points
- PCH can alert EC to out of range temperature conditions
 - TEMP_ALERT# signal assertion

Byte	Data	Format	Units	Range
0	Max. Package Temperature	Unsigned byte	1°C/bit	0-255°C
1	PCH Temperature	Unsigned byte	1°C/bit	0-255°C
3:2	CPU Temperature	10.6 Format	1/64°C/bit	0-256°C
4	MCH Temperature	Unsigned byte	1°C/bit	0-255°C
5	DIMM0 Temperature	Unsigned byte	1°C/bit	0-255°C
6	DIMM1 Temperature	Unsigned byte	1°C/bit	0-255°C
7	DIMM2 Temperature	Unsigned byte	1°C/bit	0-255°C
8	DIMM3 Temperature	Unsigned byte	1°C/bit	0-255°C
9	Sequence Number	Unsigned byte	Count	0-255
13:10	CPU Energy Counter	16 int:16frac	0.125J/bit	N/A
19:14	Host Status	Status register	N/A	N/A

EC-PCH Write Commands

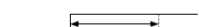
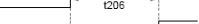
Commands	Format	Units
SMBus Turbo Status (STS)	Register	
CPU Temperature Limits	10.6 Format	1/64°C/bit
MCH Temperature Limits	Unsigned byte	1°C/bit
IBX Temperature Limits	Unsigned byte	1°C/bit
DIMM Temperature Limits	Unsigned byte	1°C/bit
Processor Power Clamp	Unsigned word	0.1W/bit

IBEXPEAK - M (DMI,FDI,GPIO)

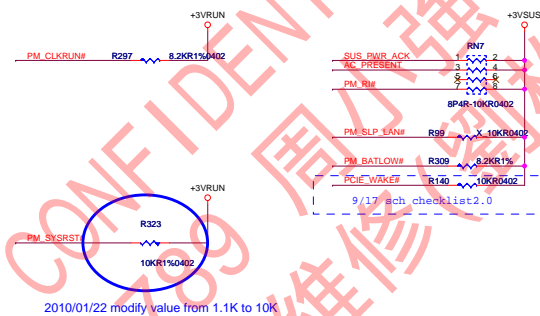


Flexible Display Interface

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibex Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP_INT is used for interrupts from sink (Ibex Peak) to source (Havendale).

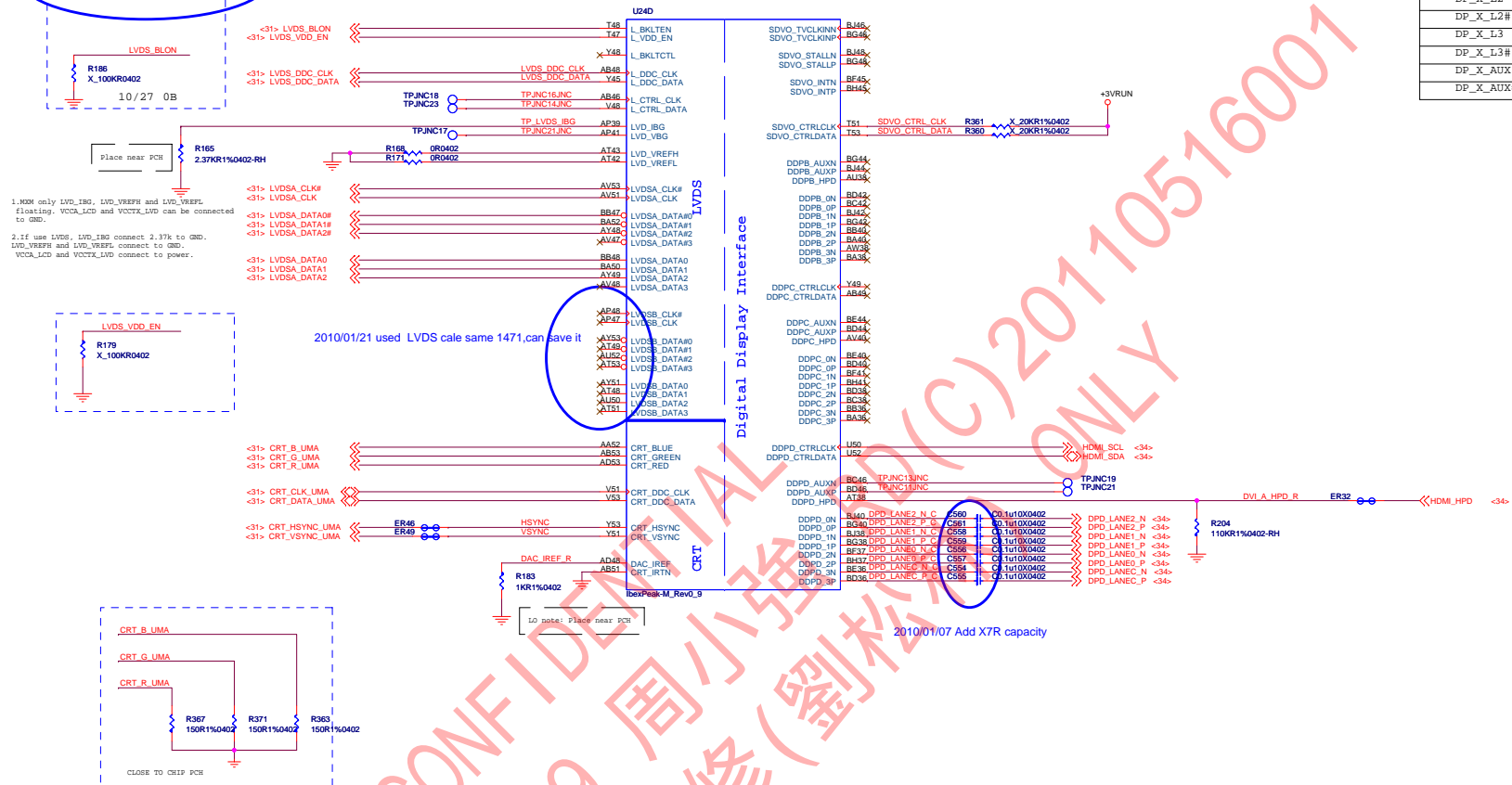
Source	Dest	Signal Name				
Board	PCH	PWROK				
PCH	Processor	DRAMPWRGD				
PCH	Processor	PROCPWRGD				
Sym	Parameter		Min	Max	Units	Notes
t209	PWROK active to PROCPWRGD active		See Note 7	—	ms	7
t206	PWROK deglitch time		1	—	ms	6

6. Ensure PWROK is a solid logic '1' before proceeding with the boot sequence. Note: If PWROK drops after t206 it will be considered a power failure.
7. t209 minimum timing selectable as 1 ms (recommended), 5 ms, 50 ms, or 100 ms using bits 9:8 of PCHSTRP15.



2010/01/22 remove component to save layout space

IBEXPEAK - M (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

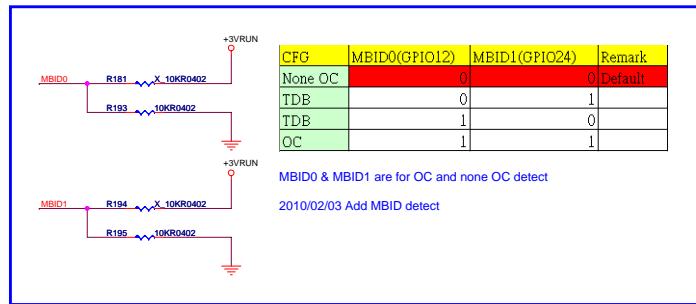
2010/02/03 Add MBID detect

Table 8-4. Measured I/O voltage rails

Voltage Rail	Voltage (V)	Source
V_CPU_IO	1.1/1.05	50% Cn Int Gr
V5REF	5	
V5REF_Sus	5	
Vcc3_3	3.3	
VccADAC	3.3	
VccADPLL	1.05	
VccADPLLB	1.05	
VccCore	1.05	
VccDMI	1.1	
VccIO	1.05	
VccLAN	1.05	
VccME	1.05	
VccME3_3	3.3	
VccpNAND	1.8	
VccRTC	3.3	
VccSus3_3	3.3	
VccSusHDA	3.3	
VccVRM	1.8/1.5	
VccALVDS	3.3	
VccTX_LVDS	1.8	

SKU	Thermal Design Power (TDP)	Notes
QM57	3.5 W	1
HM57	3.5 W	1
HM55	3.5 W	1
PM55	3.5 W	1
QS57	3.4 W	1

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/1.05	.001	.001	.001	.001			—
V5REF	5	.001	.001	.001	.001			—
V5REF_Sus	5	.001	.001	.001	.001	.001		—
Vcc3_3	3.3	.305	.305	.0176	.0176			—
VccADAC	3.3	.075	.0011	.0011	.0011			—
VccADPLLA	1.05	.088	.0176	.825	.0044			—
VccADPLLB	1.05	.088	.0176	.0044	.0044			—
VccCore	1.05	1.43	1.254	.3685	.2805			—
VccDMI	1.1	.055	.055	.0011	.0011			—
VccIO	1.05	3.23	2.628	.463	.285			—
VccLAN	1.05	.220	.220	.066	.066	.132		—
VccME	1.05	1.2	1.2	.186	.186	.98	.0044	—
VccME3_3	3.3	.031	.031	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022			—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.087	.087	.0132	.0132	.133	.0297	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.156	.114	.113	.045			—
VccALVDS	3.3	.0011	.0011	.0011	.0011			—
VccTX_LVDS	1.8	.066	.0011	.0198	.0011			—

IBEXPEAK - M (POWER)



IBEXPEAK - M (GND)



Intel® 5 Series Chipset Mobile SKUs

Feature Set	SKU Name(s)				
	QM57	HM57	PM55	HM55	QSS7
PCI Express* 2.0 Ports	8	8	8	6 ⁵	8
USB* 2.0 Ports	14	14	14	12 ⁴	14
SATA Ports	6	6	6	4 ⁶	6
HDMI/DVI/VGA/SDVO/DisplayPort	Yes	Yes	No	Yes	Yes
LVDS	Yes	Yes	No	Yes	Yes
Graphics Support with PAVP 1.5	Yes	Yes	No	Yes	Yes
FIS Based Port Multiplier Support	Yes	Yes	Yes	No	Yes
Intel® Quiet System Technology	No	No	No	No	No
Intel® Rapid Storage Technology	Yes	Yes	Yes	Yes	Yes
AHCI	Raid 0/1/5/10 Support	Yes	Yes	No	Yes
Intel® ME Ignition FW only	No	No	Yes	No	No
Intel® AT	Yes	Yes	No	Yes	Yes
Intel® AMT 6.0	Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Business	Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Consumer	No	Yes	No	No	No
Intel® Remote Wake Technology	No	No	No	No	No

Figure 2-6. Platform Power Block Diagram—S3, M-Off, with WoL, No WoWLAN

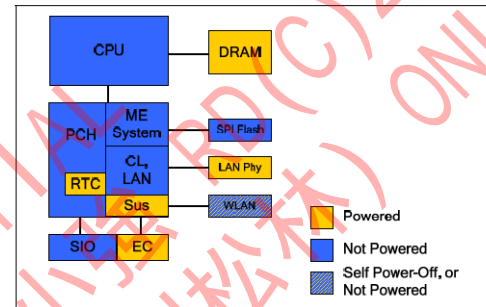


Figure 2-9. Platform Power Block Diagram—S4-S5, M-Off, with WoL, No WoWLAN

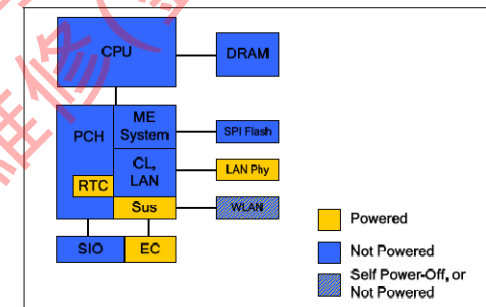
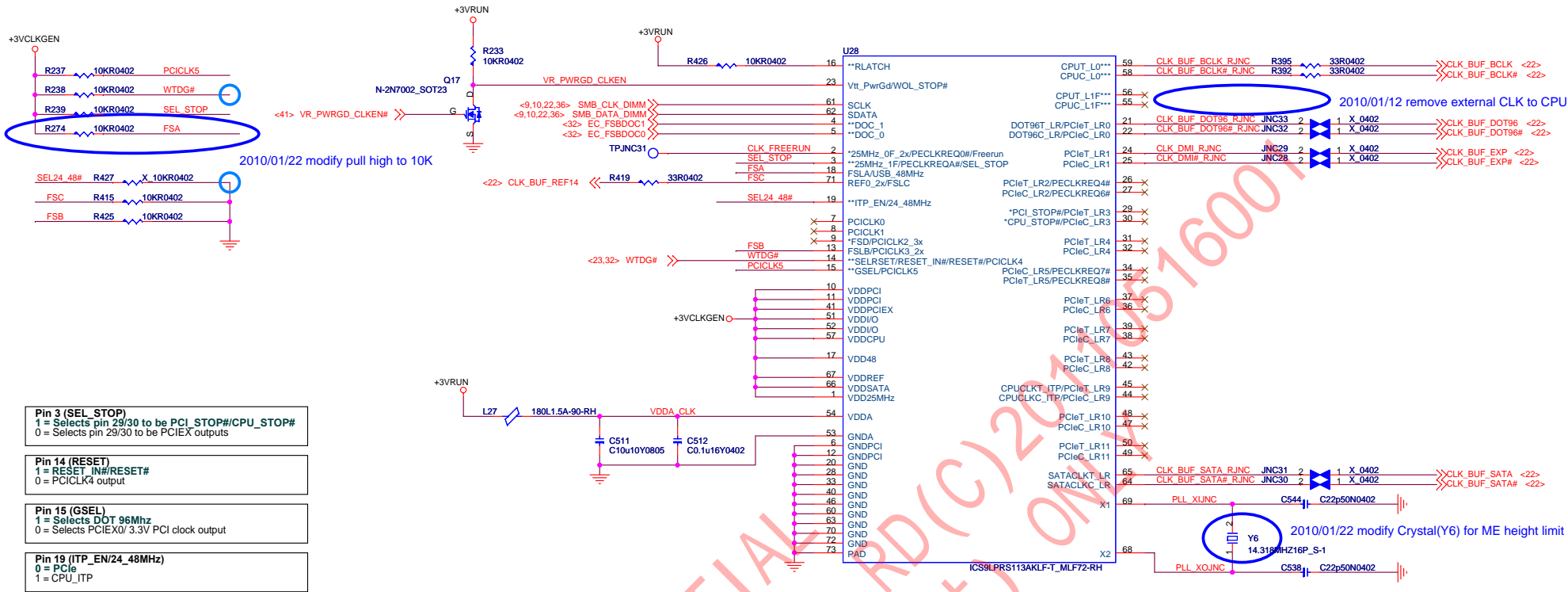
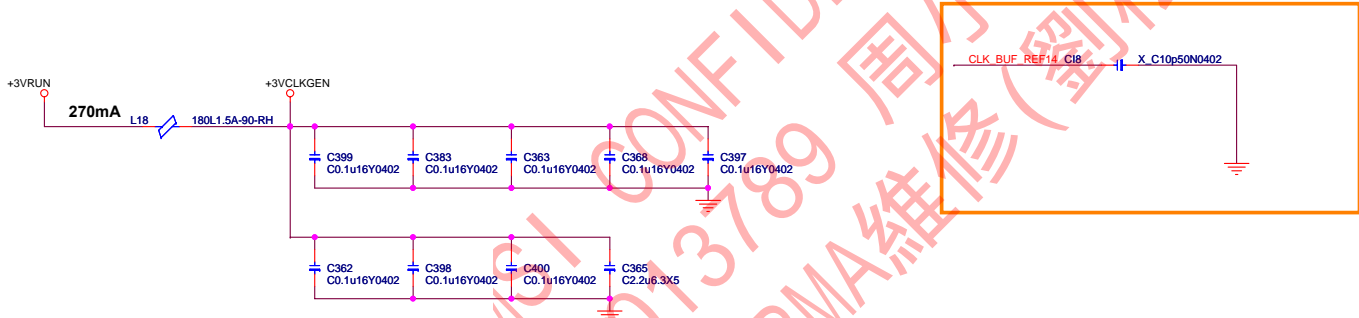


Table 113. Power Delivery Summary for Intel Management Engine SubSystem (Sheet 1 of 2)

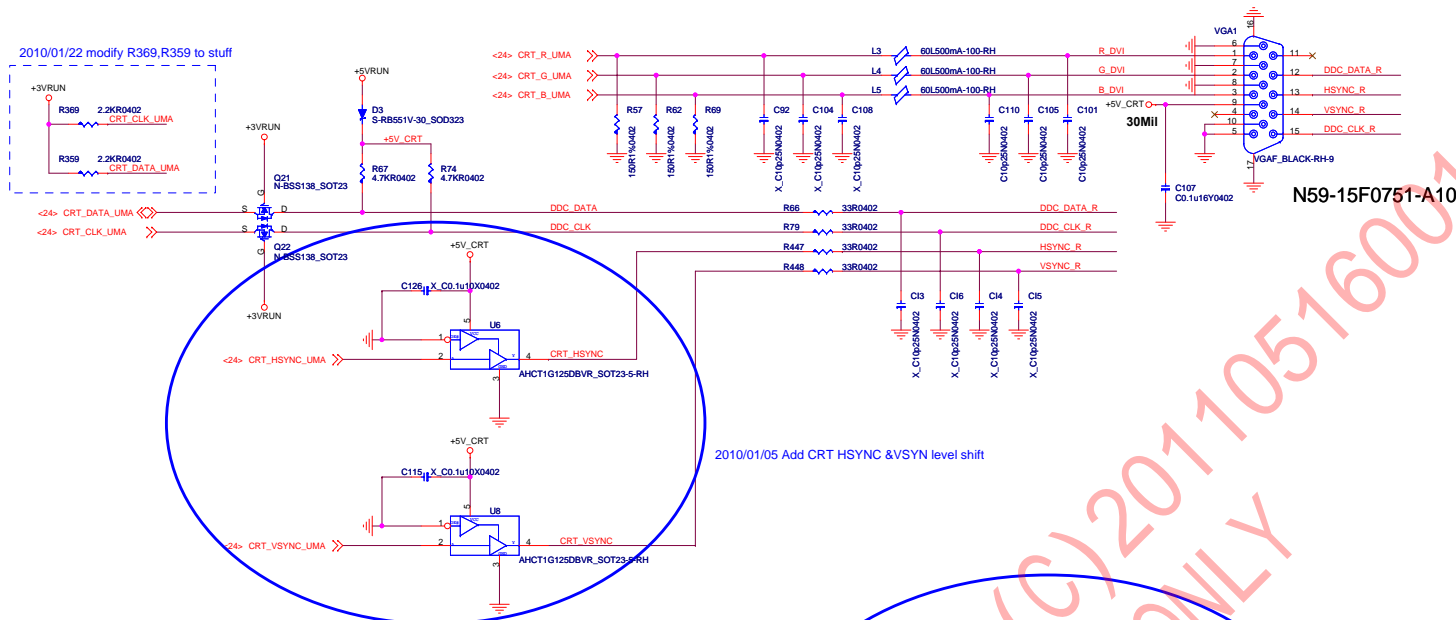
What It Powers	Rail	Sx ¹ /M3	Sx/Moff ²	Sx/Moff/WOL ³	Source	Enabled By	Power OK indicator
Platform 5-V Rail	V5.0A	On	On	On	5 V Always (Sx)		
DRAM VDD	V1.5U	On in S3	On in S3	On in S3	V1.5U	SLP_S4#	
DRAM VTT	V0.75S or V0.75U	Off ⁴	Off ⁴	Off ⁴	V0.75S or V0.75U	SLP_S3#	
CK50S	3.3 CK50S	Off ⁵	Off ⁵	Off ⁵	V3.3S	CKPWRGD	
Mobile Intel® 5 Series Chipset	1.05 VCORE	Off ⁵	Off ⁵	Off ⁵	V1.05S		PWROK
WLAN	V3.3A	On	On	On	3.3 V Always		
M3 Support + Intel® 82577 GbE LAN							
Intel® ME Local RAM	V1.05M	On	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	On	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	On	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN controller	VCCLAN	On	Off	Off	V1.05M	SLP_M# ⁶	
No M3 Support + Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M	Off	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	Off	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	V1.05M	SLP_M# ⁶	
No M3 Support + No Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M/1.1M	Off	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		



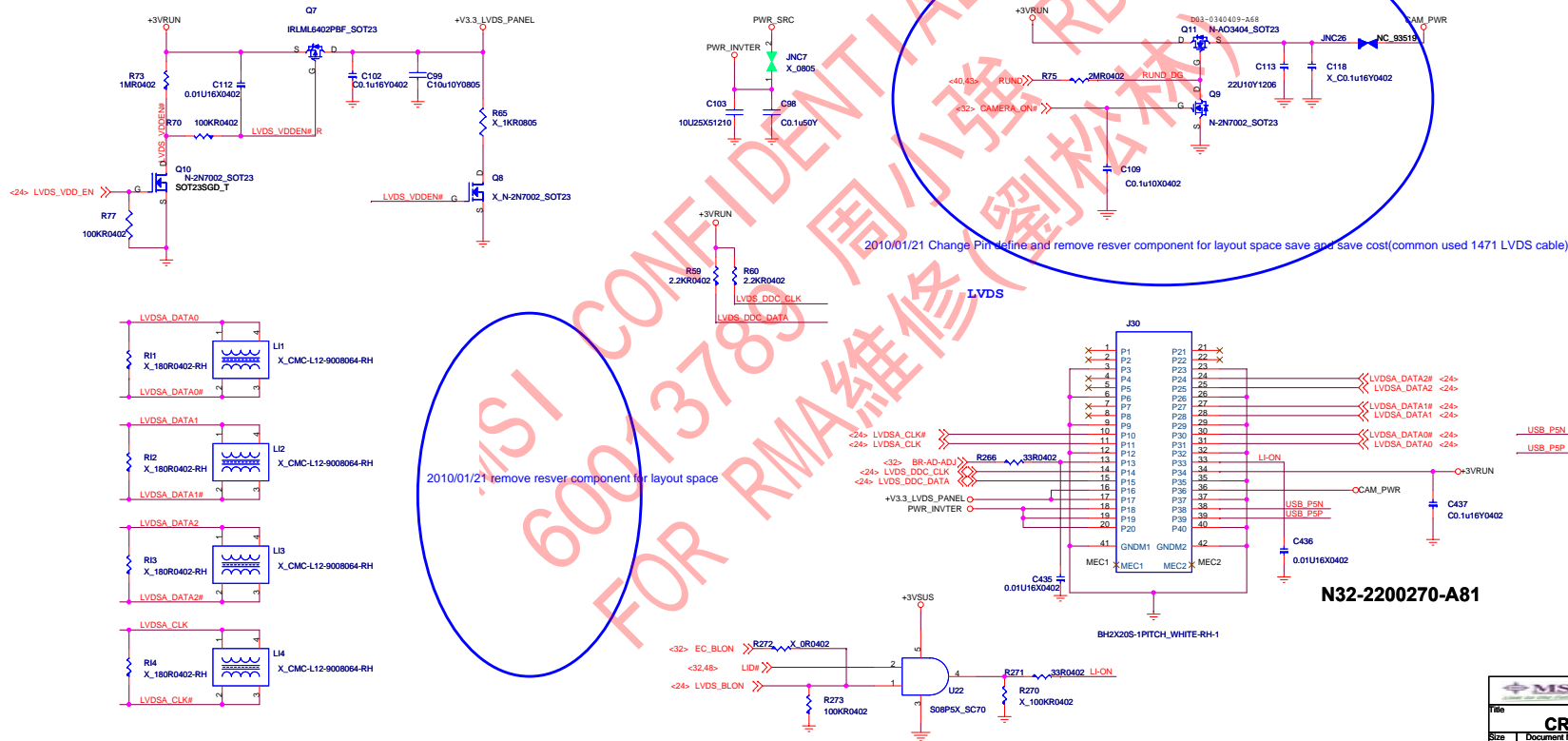
- Pin 3 (SEL_STOP)**
1 = Selects pin 29/30 to be PCI_STOP#/CPU_STOP#
0 = Selects pin 29/30 to be PCIe_X outputs
- Pin 14 (RESET)**
1 = RESET_IN#/RESET#
0 = PCICLK4 output
- Pin 15 (GSEL)**
1 = Selects DOT 96Mhz
0 = Selects PCIe_X/ 3.3V PCI clock output
- Pin 19 (ITP_EN/24_48MHz)**
1 = CPU_ITP

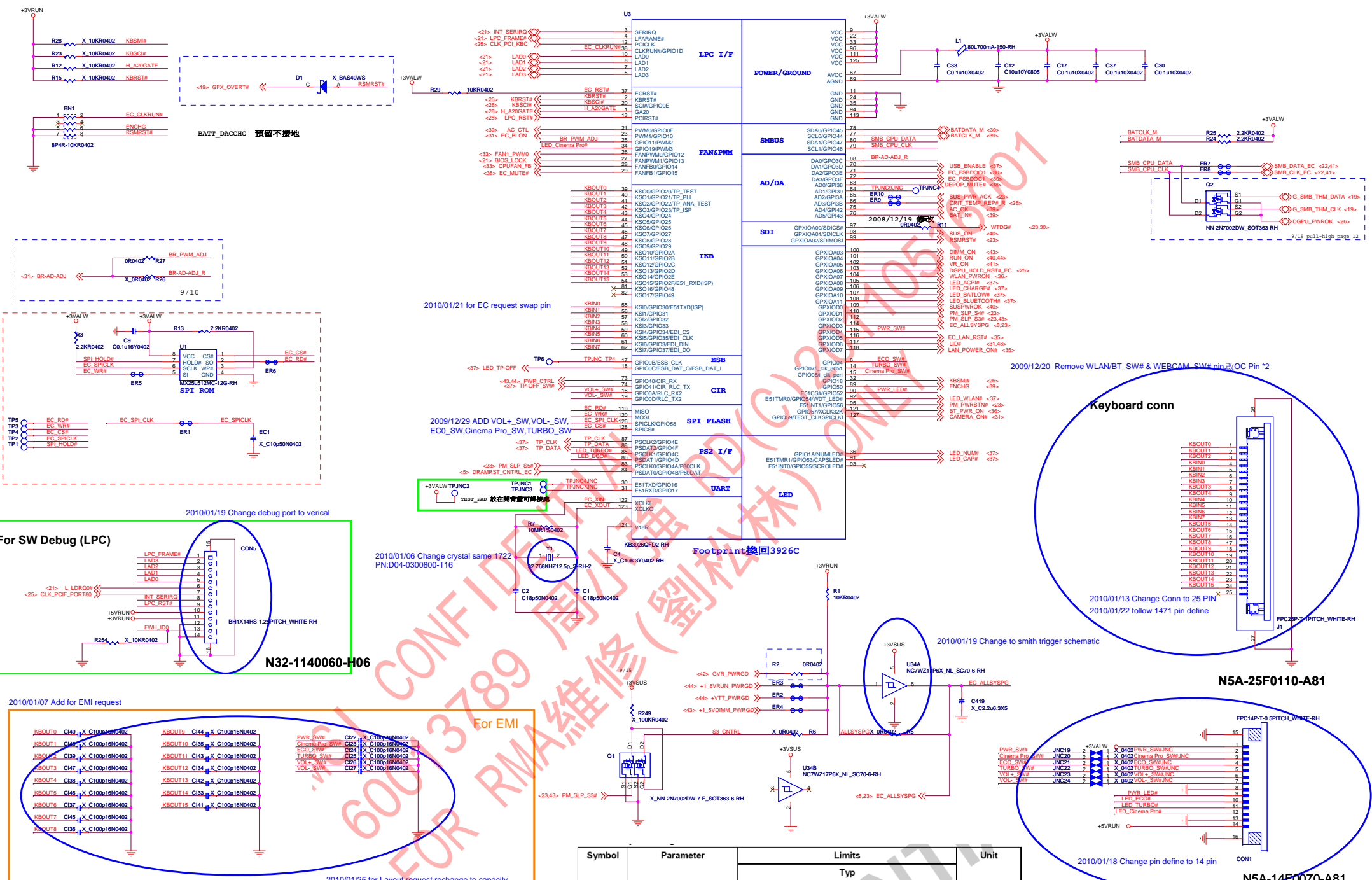


CRT



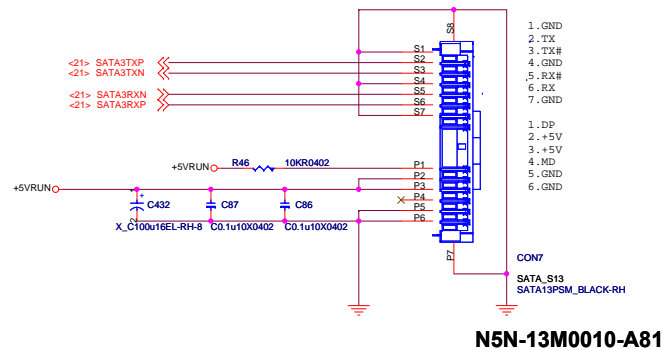
LVDS



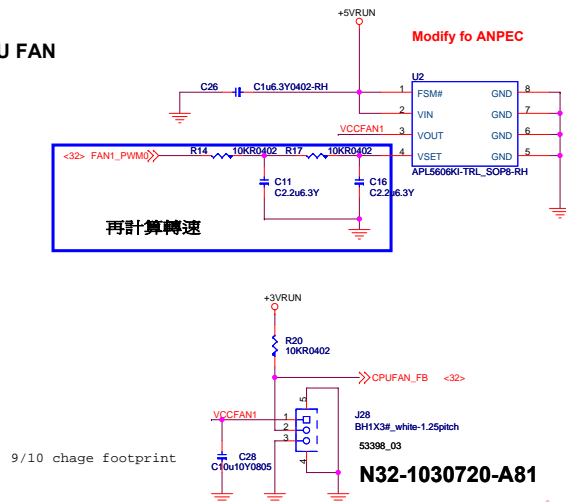


Symbol	Parameter	Limits	Unit
		Typ	
Icc	Typical current consumption in operating state under Windows environment. All clock domains are running, and no keyboard/mouse activities.	20	mA

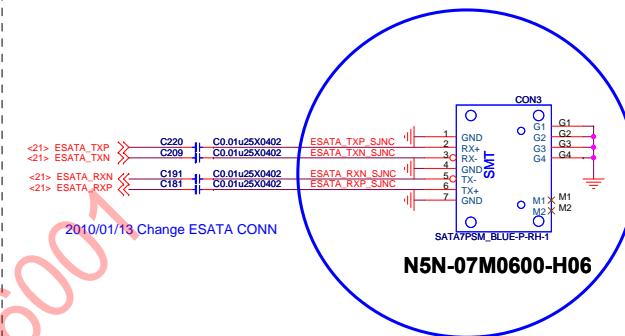
SATA ODD



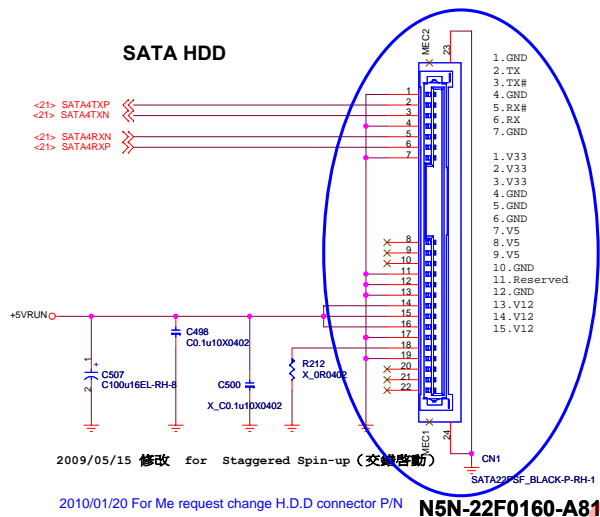
CPU FAN



ESATA

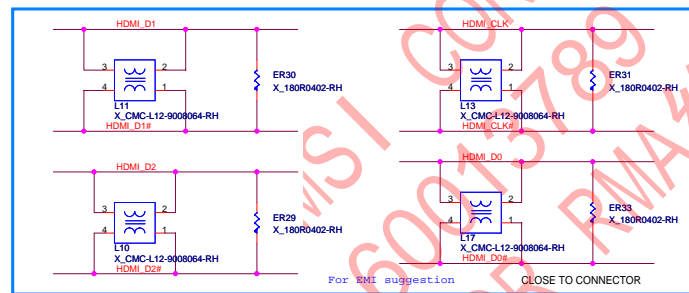
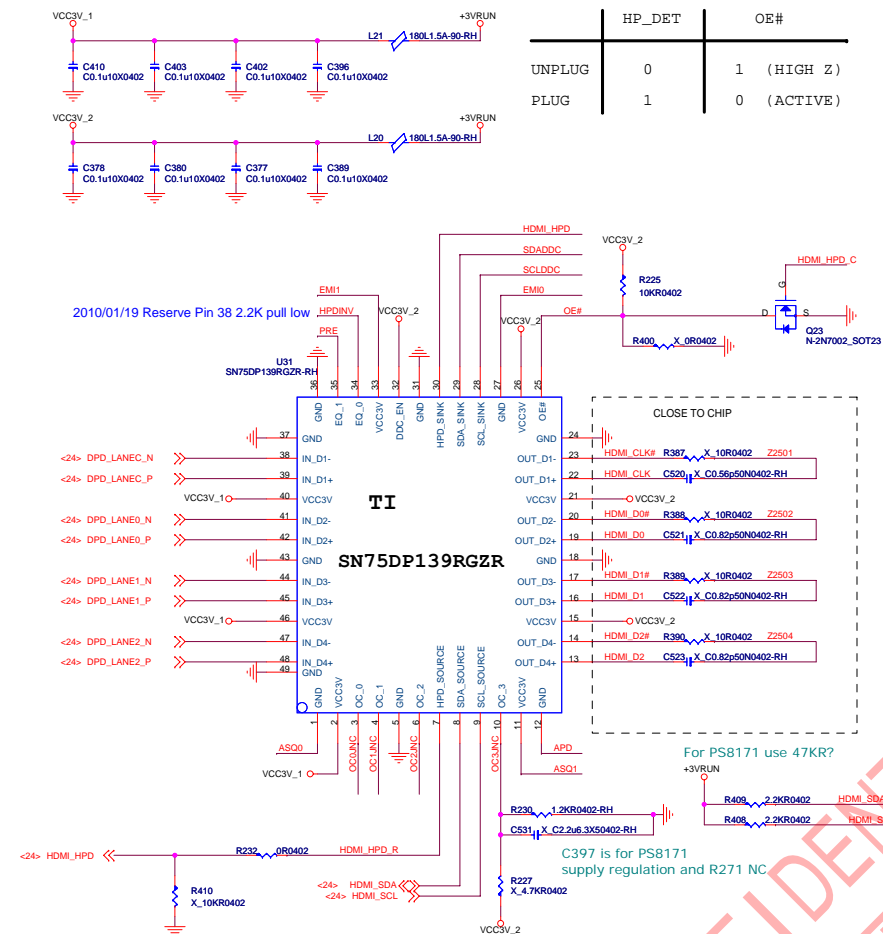


SATA HDD

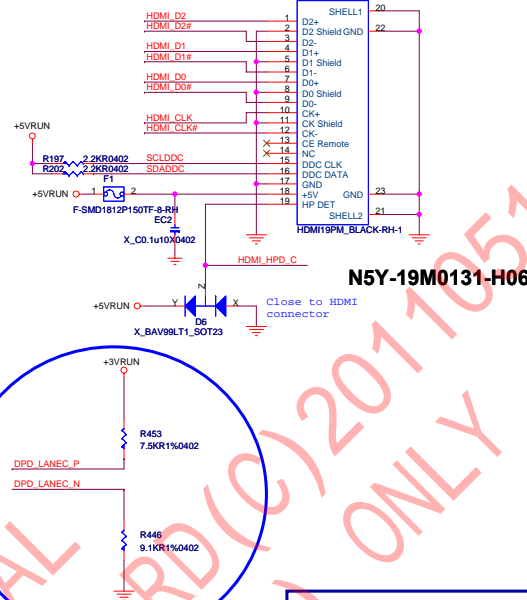


MSI MICRO-STAR INT'L CO.,LTD.			
Title			
ODD,HDD,ESATA,FAN			
Size	Document Number	Rev	
Custom	MS-1481	0A	
Date:	Sheet	33	of 56

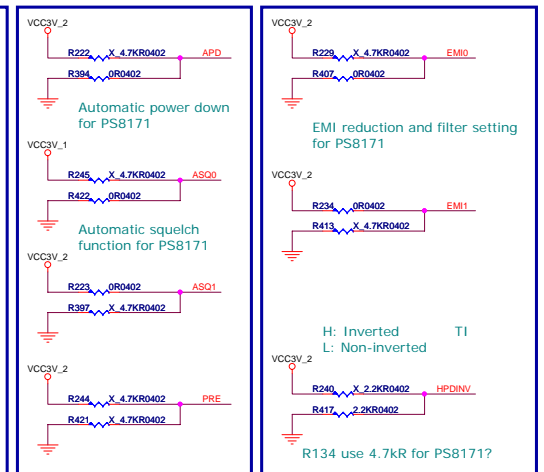
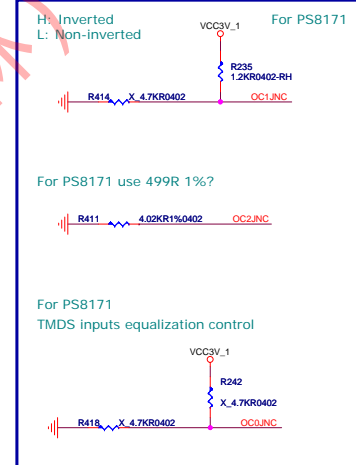
HDMI Switch



HDMI connector



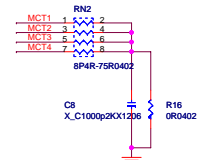
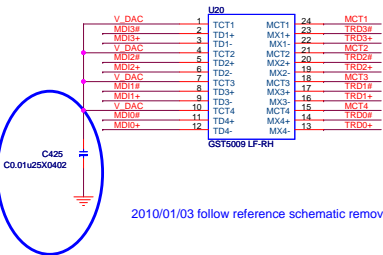
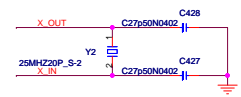
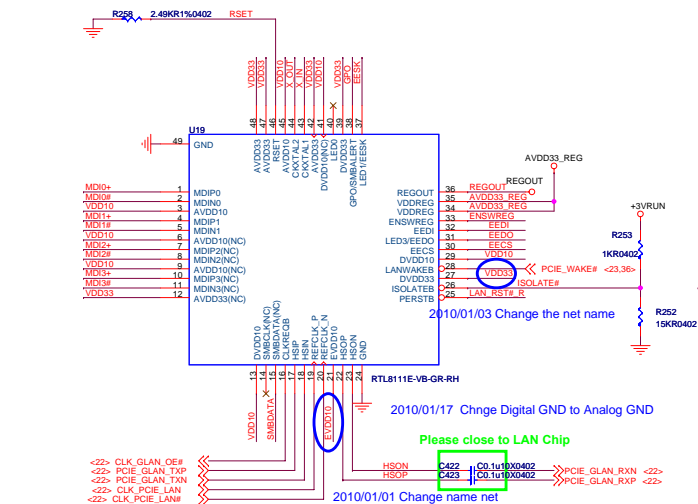
2010/01/29 Add for TI suggestion



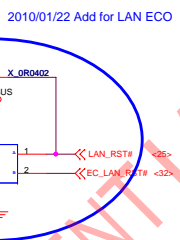
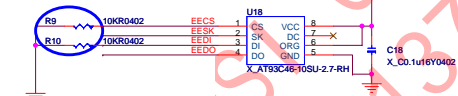
SN75DSP139	PS8171	Pin no.
Floating	<p>TMDS inputs equalization control (internal pull-down~500kΩ)</p> <p>PEQ = LOW: Mid level EQ (Default)</p> <p>PEQ = HIGH: High level EQ</p> <p>PEQ = MID: Low level EQ</p>	Pin 3
High	<p>(Internal pull down~500kΩ)</p> <p>PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output</p> <p>PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.9V</p>	Pin 4
GND	<p>[ASQ1,ASQ0] = HL: No automatic squelch (Internal pull down~500kΩ)</p> <p>LL: Automatic squelch enable, Level = 120mVpp, default timer</p> <p>LH: Automatic squelch enable, Level = 100mVpp, default timer</p> <p>HH: Automatic squelch enable, Level = 80mVpp, default timer</p> <p>ML: Automatic squelch enable, Level = 120mVpp, extended timer</p> <p>MH: Automatic squelch enable, Level = 100mVpp, extended timer</p> <p>LM: Automatic squelch enable, Level = 80mVpp, extended timer</p> <p>HM: Reserved</p> <p>MM: Reserved</p>	Pin 1
VCC		Pin 11
4.68K to GND	499R to GND	Pin 6
GND	<p>Automatic power down management (Internal pull up~500kΩ)</p> <p>APD = LOW: Automatic power down disable</p> <p>APD = HIGH: Automatic power down enable</p> <p>APD = MID: Reserved</p>	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	<p>EMI reduction and filter setting.</p> <p>(EMI1 Internal pull up~500kΩ; EMI0 Internal pull down~500kΩ)</p> <p>(EMI1,EMI0) = HL: No EMI reduction</p> <p>EMIO = HIGH: Reduced rise/fall time</p> <p>MID: Reduced rise/fall time, 2nd</p> <p>EMI1 = LOW: EMI filter setting 1</p> <p>MID: Reserved</p>	Pin 27
VCC		Pin 33
Note2	<p>DDC Active Buffer enable and setting (internal pull-down~500kΩ)</p> <p>DDC8BUF = LOW: No DDC active buffer, passive DDC level shifting</p> <p>DDC8BUF = HIGH: Active DDC buffer enable, setting 1</p> <p>DDC8BUF = MID: Active DDC buffer enable, setting 2</p>	Pin 34
Floating	<p>TMDS output driver pre-emphasis level setting (internal pull down~500kΩ)</p> <p>PRE = LOW No pre-emphasis</p> <p>PRE = HIGH: Low level pre-emphasis is added</p> <p>PRE = MID: High level pre-emphasis is added</p>	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted

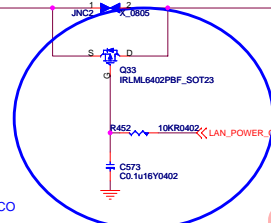
Note: add 0.1u cap at each power pin of LAN, please don't save.



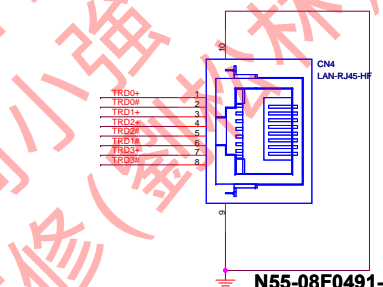
2010/01/04 follow reference schematic add 10K pull low



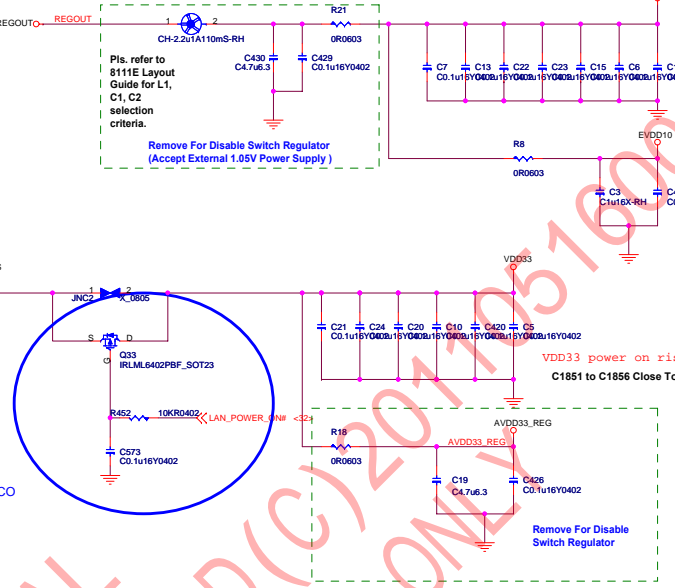
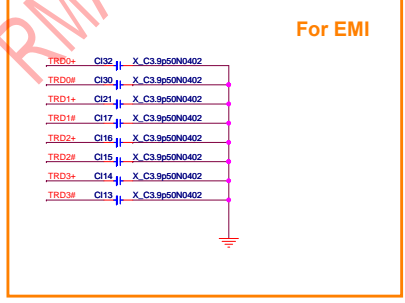
2010/01/22 Add for LAN ECO



2010/01/22 Add for LAN ECO

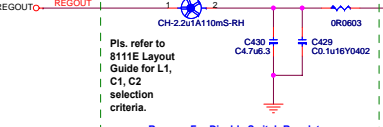


For EMI



Use External 1.05V Supply When Disable Switch Regulator.
If Using External 1.2V Supply Pls. Contact With FAE.

2010/01/08 remove it, if used jump write



Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

2010/01/22 Add for LAN ECO

VDD33 power on rise time >1ms
C1851 to C1856 Close To LAN chip

Remove For Disable Switch Regulator

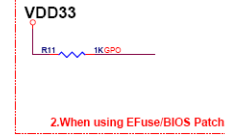
For RTL8105E
* C1841 to C1844 are for VDD10 pins-- 3, 13, 29, 45.
For RTL8111E
* C1841 to C1848 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

Part Reference	Choke1	C1840	C1846	R1662	R1668
Enable Switch Regulator					
Disable Switch Regulator	X	X	X	X	X

For RTL8105E
* C1851 to C1855 are for VDD33 pins-- 27, 39, 42, 47, 48.
For RTL8111E
* C1851 to C1856 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

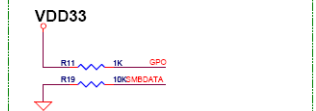
EEPROM Select

For RTL 8105E



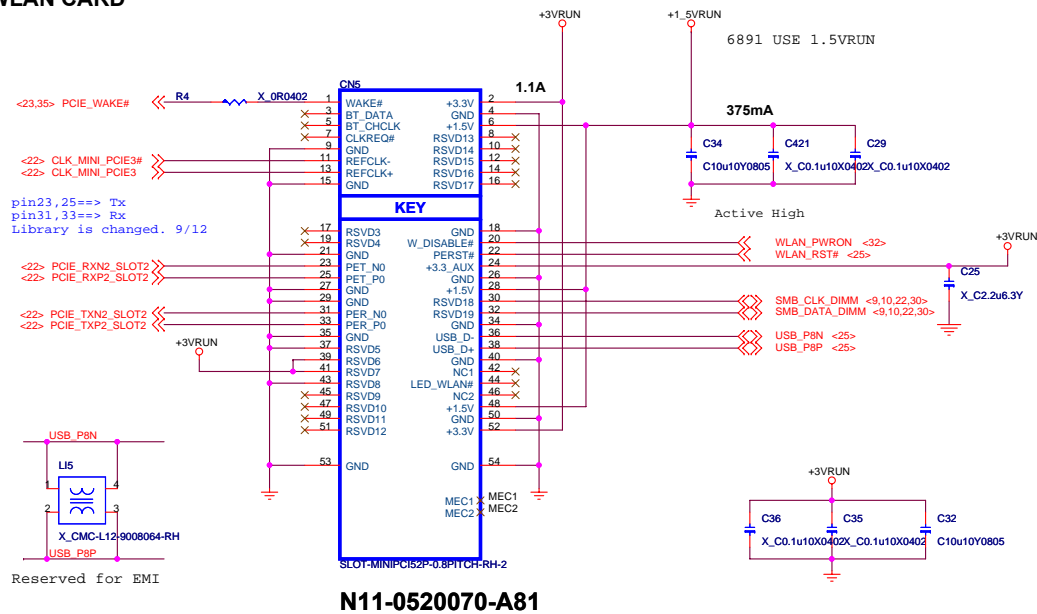
2.When using EFuse/BIOS Patch.

FOR RTL 8111E

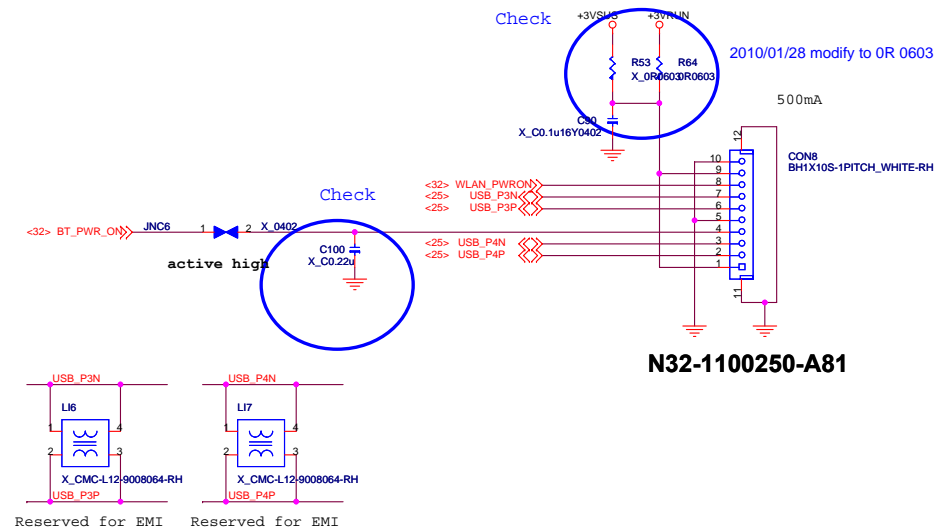


3.When using EFuse/BIOS Patch without ASF function.

WLAN CARD

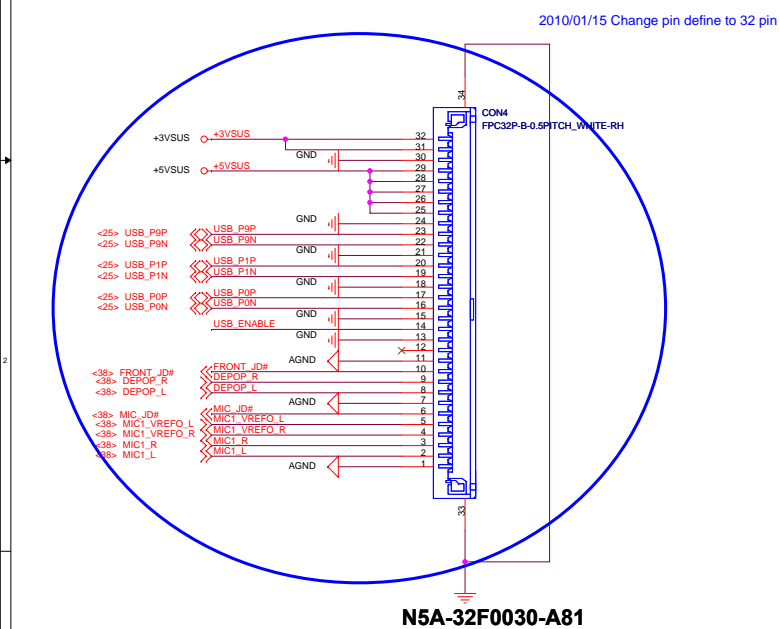
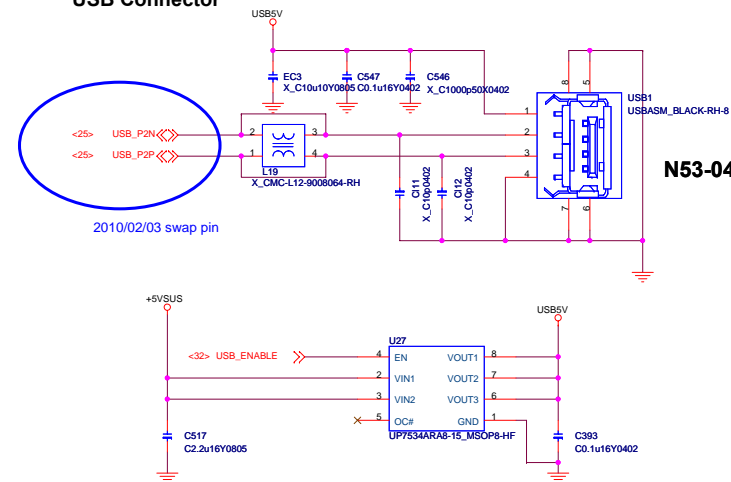
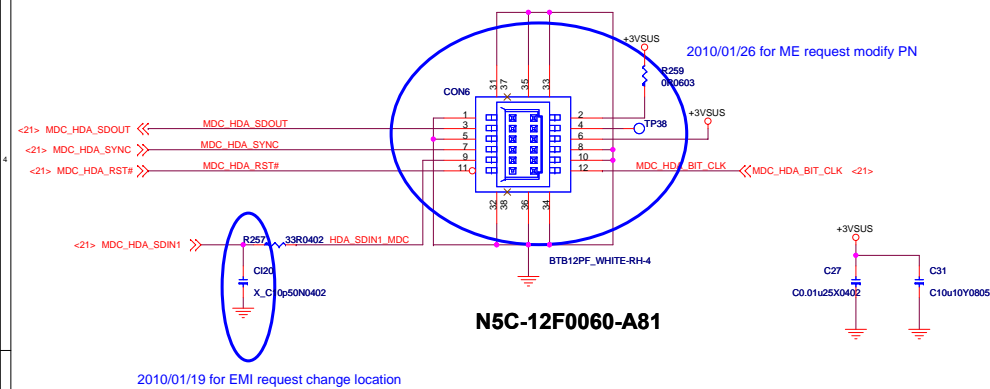


MS-3871 BT & WLAN COMBO

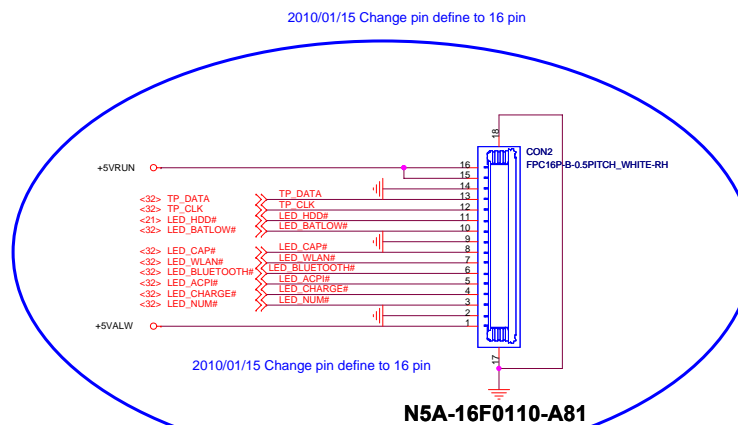


MDC

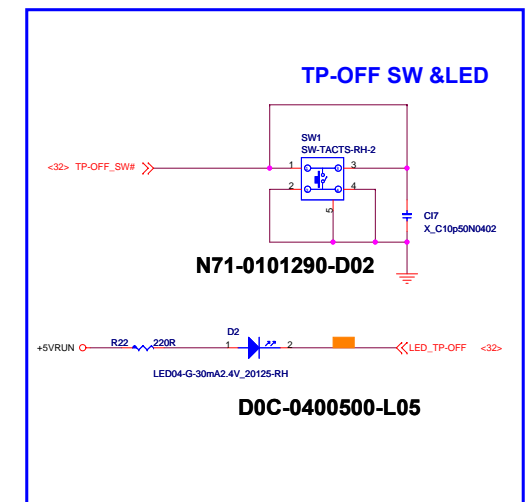
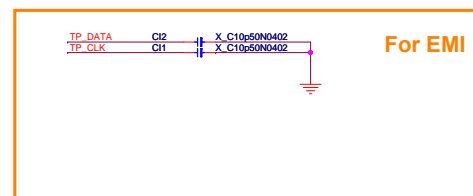
USB Connector



Connector to P.44 Board A

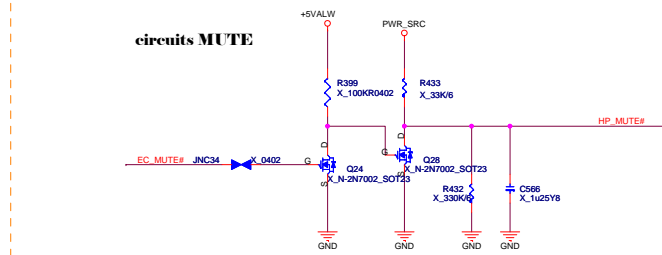
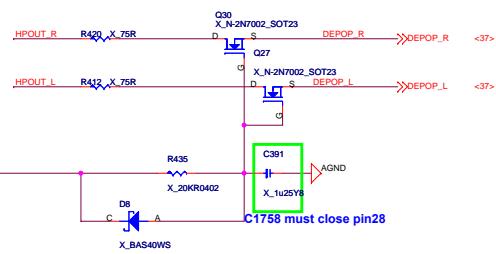
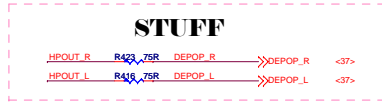
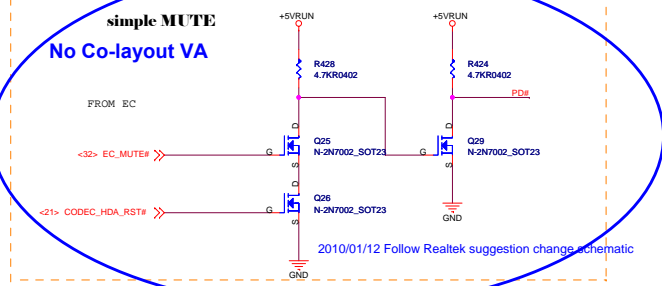
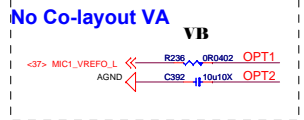
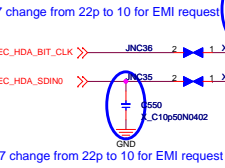
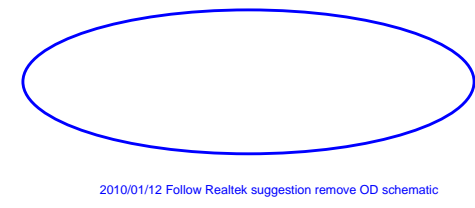
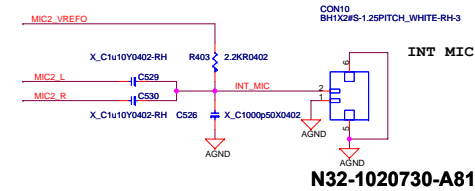
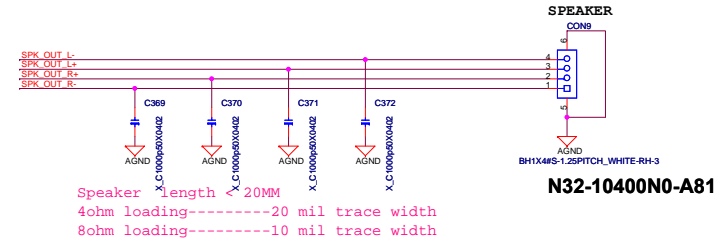
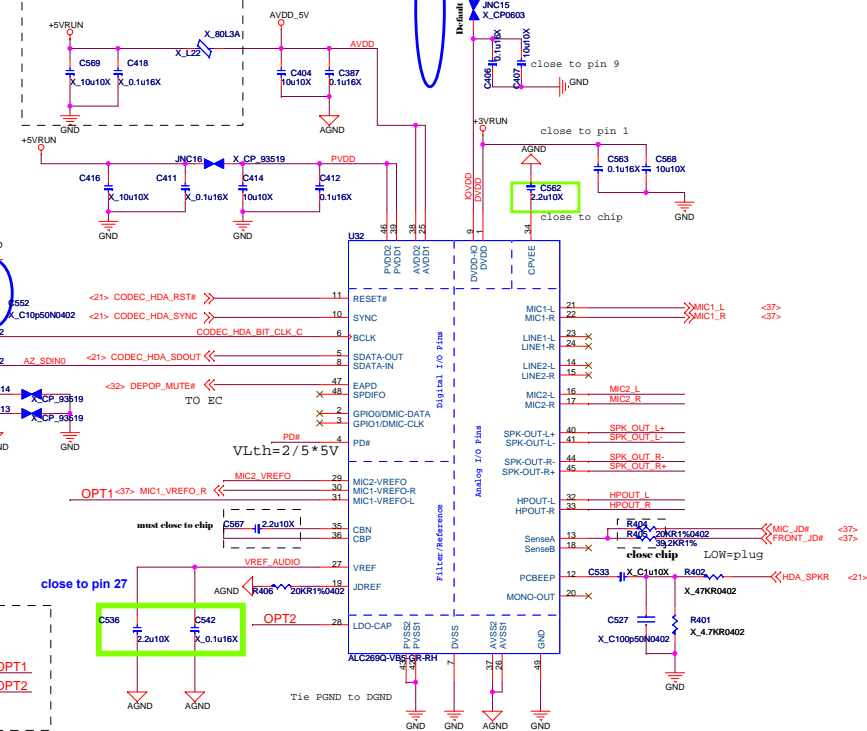


Connector to P.46 Board C



2009/12/29 Delete +1.5V RUN

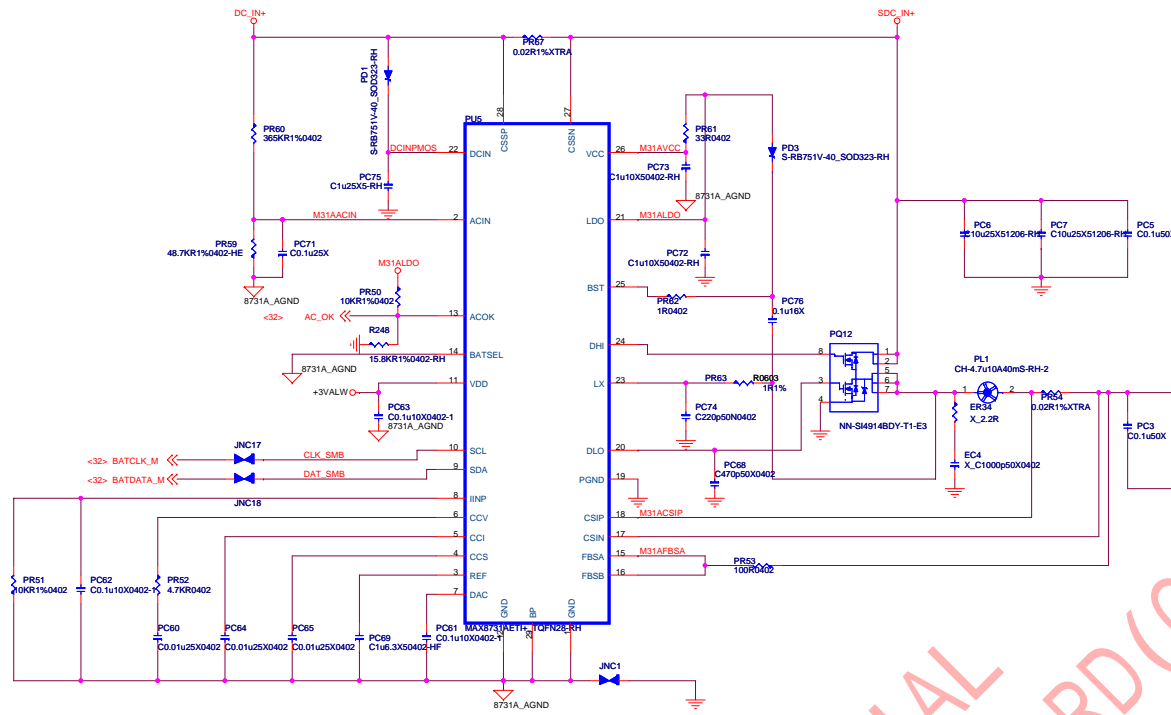
FOR ALC269-VB have internal LDO



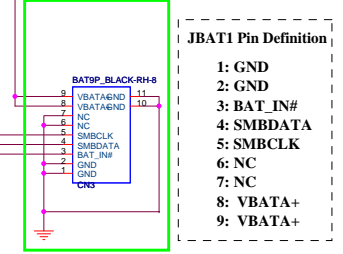
DEPOP CIRCUIT

NOT STUFF

Adapter input voltage set 19 Voltage



12/15 Change Battery Conn.



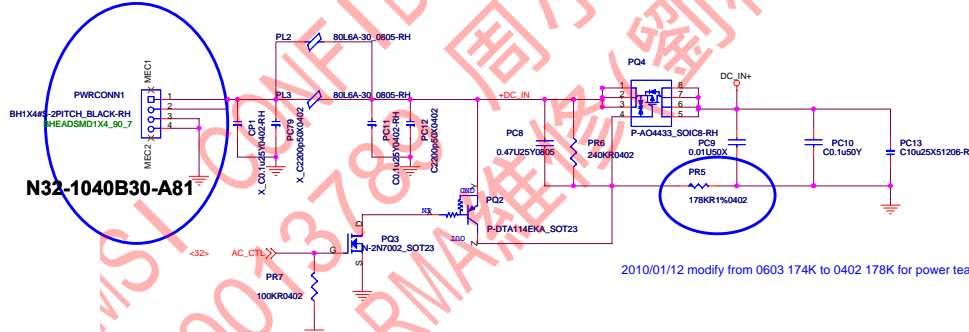
N91-09M0071-AF2

2010/01/12 Power team recommend remove

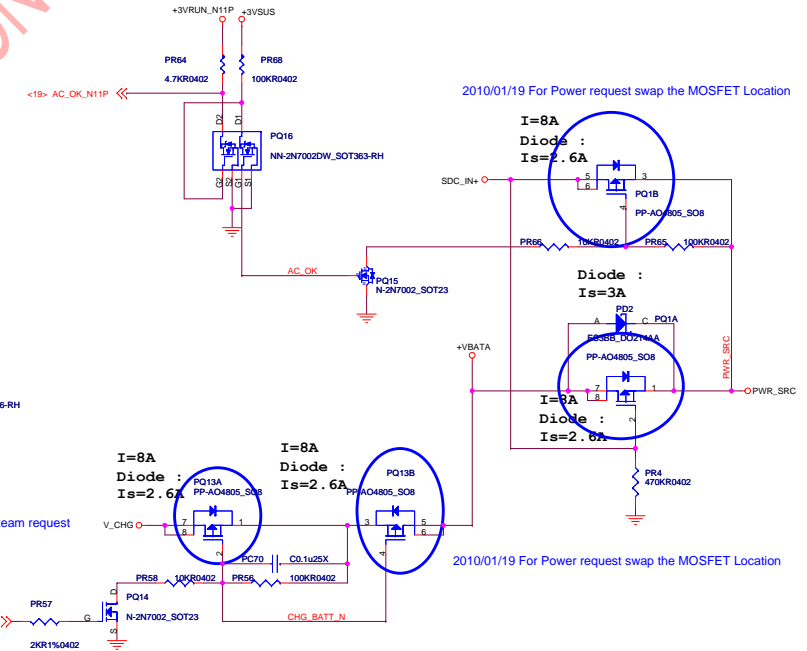
IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_IINP = IINP \times RS1 \times 3mA/V \times PR25$

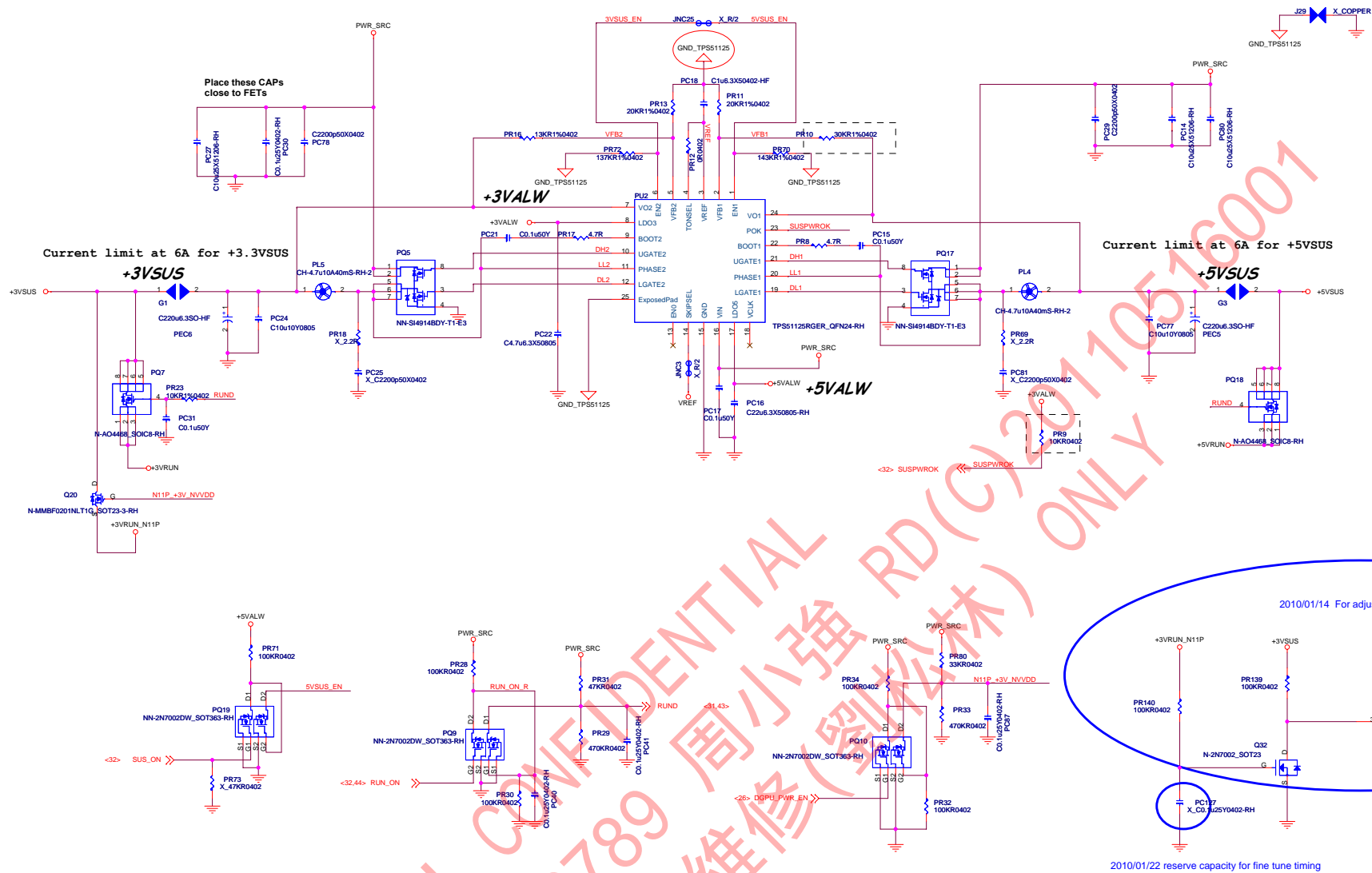
2009/12/31 更換power connector
2010/01/12 Chage connector same the 16G1

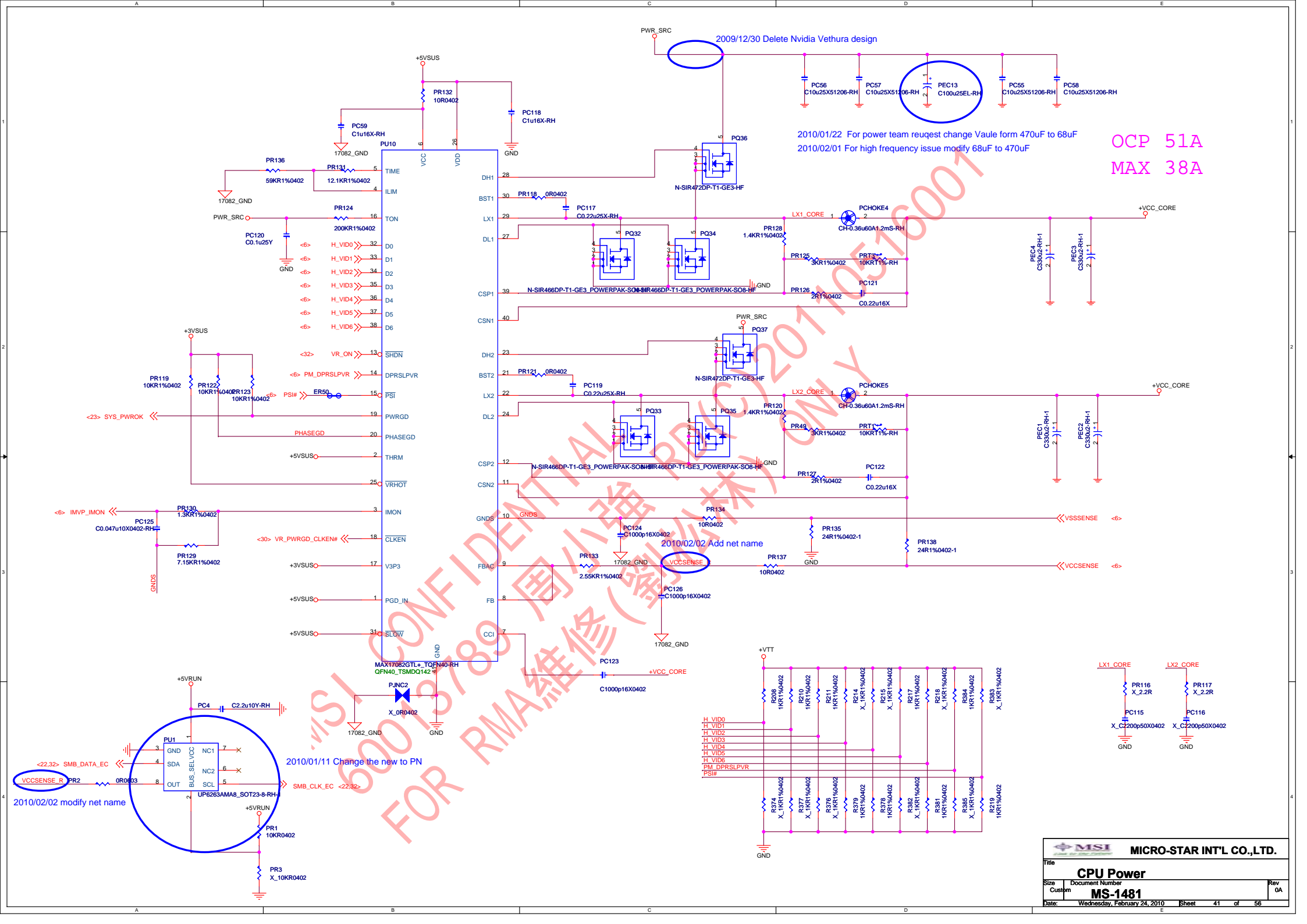


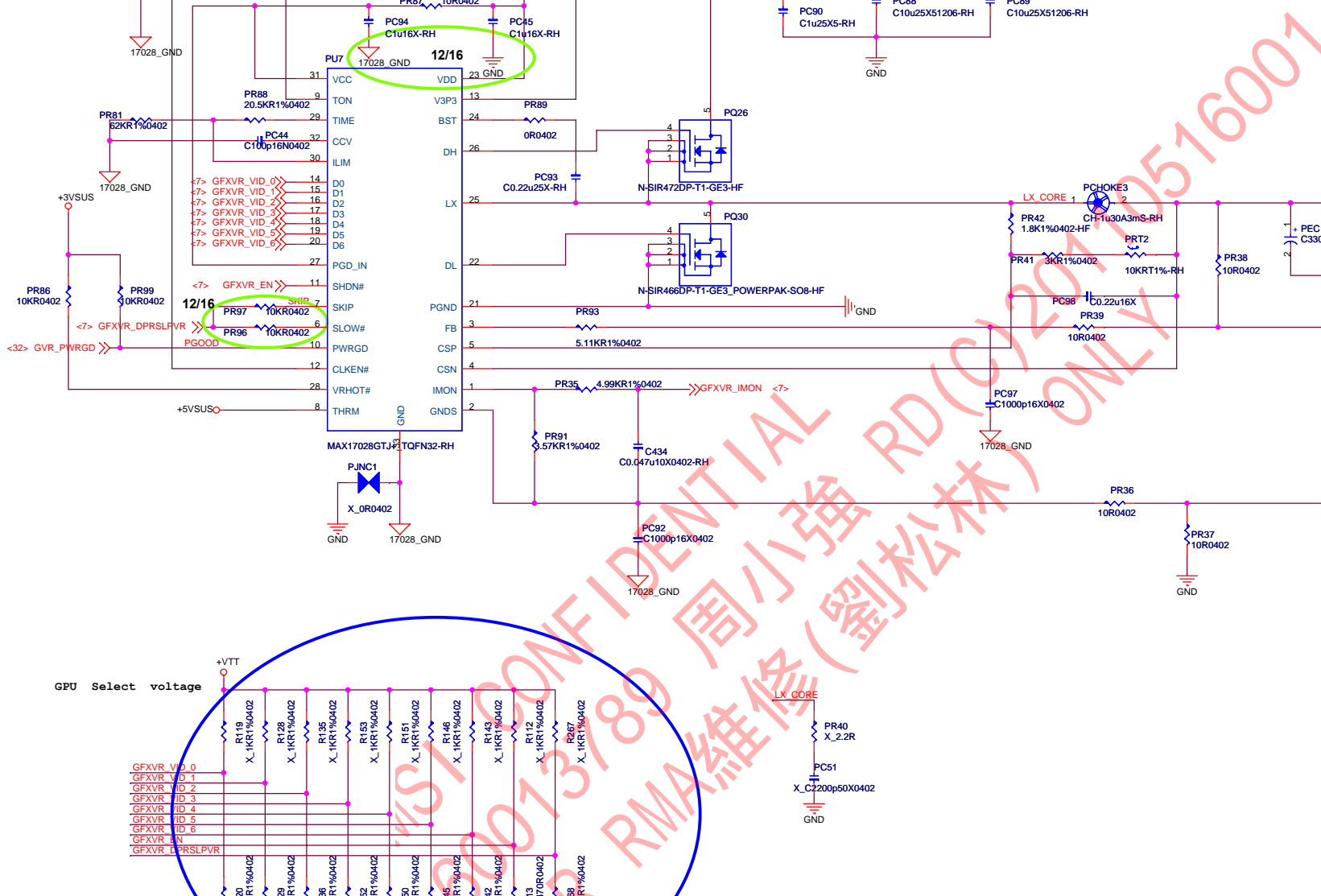
2010/01/12 modify from 0603 174K to 0402 178K for power team request

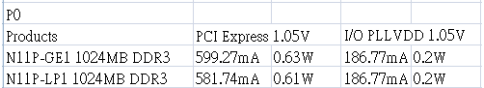


2010/01/19 For Power request swap the MOSFET Location

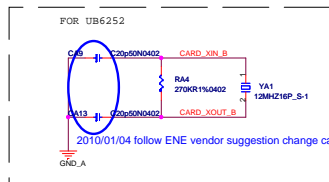




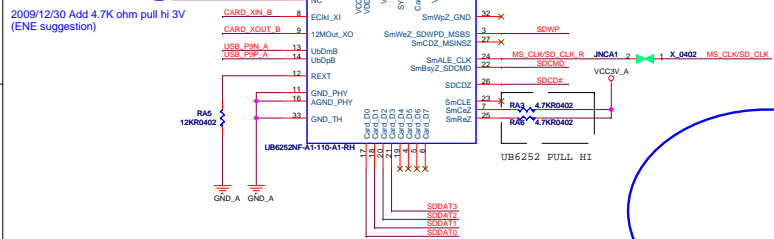




Card Reader UB6252

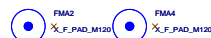
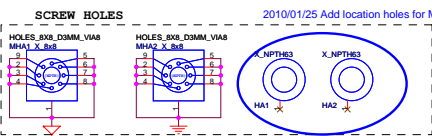


2009/12/30 Add 4.7K ohm pull hi 3V (ENE suggestion)



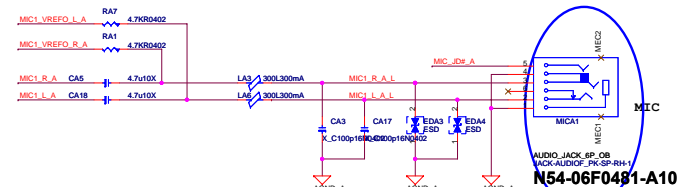
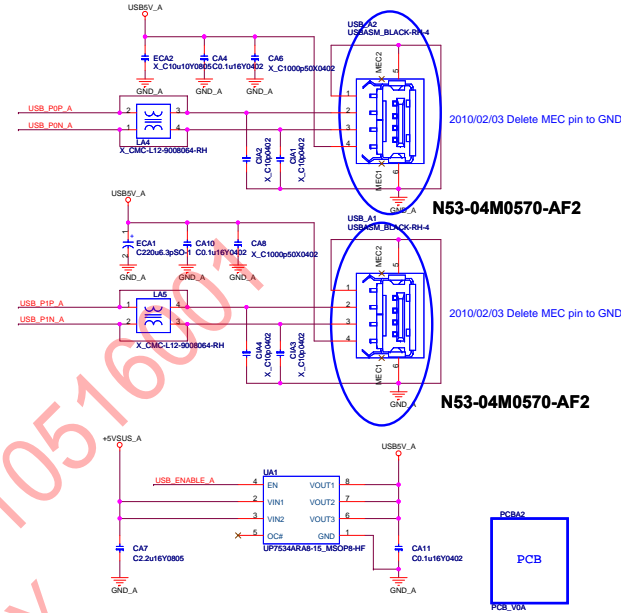
2010/01/22 modify pad size

2010/01/25 Add location holes for ME

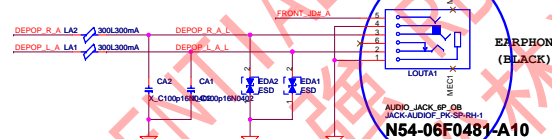


Close to socket.

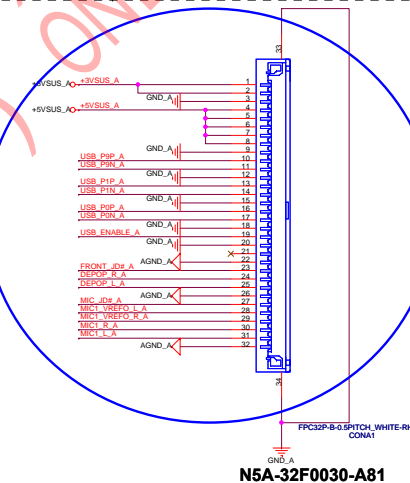
N5J-09F0110-N40



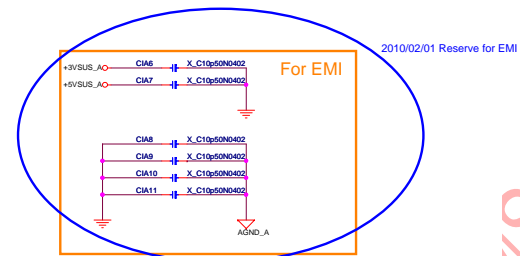
2010/02/03 modify PN to N54-06F0481-A10



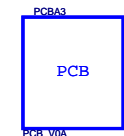
2010/02/03 modify PN to N54-06F0481-A10



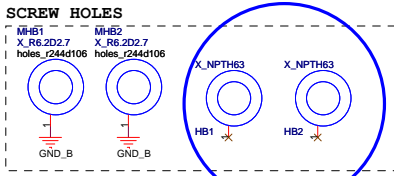
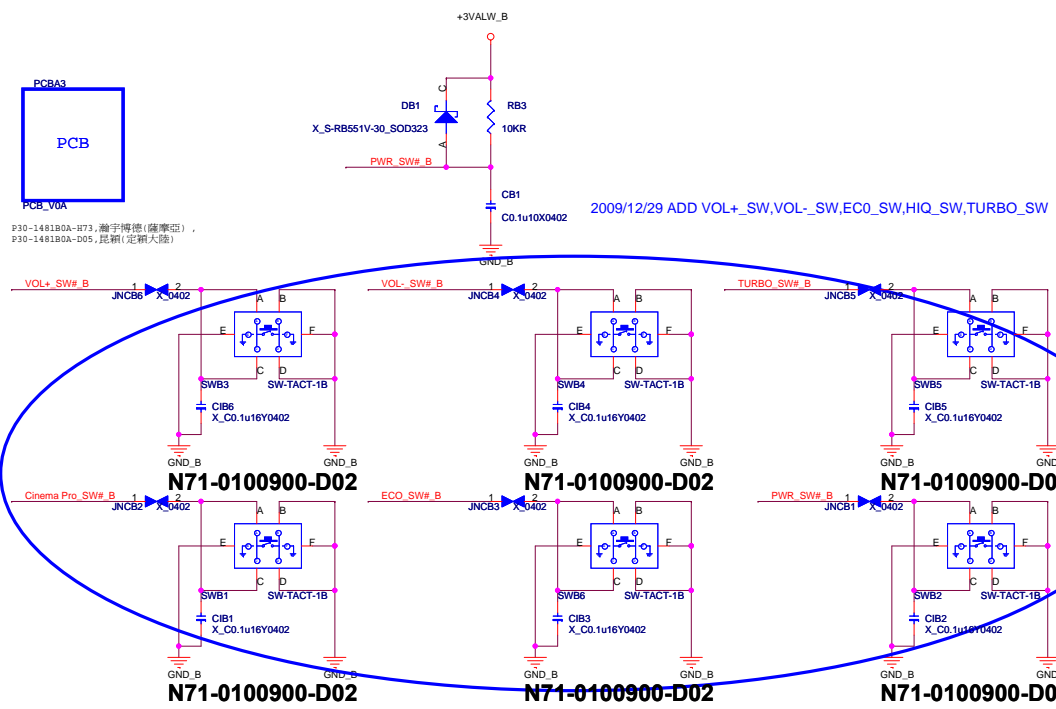
2010/01/15 Change pin define to 32 pin



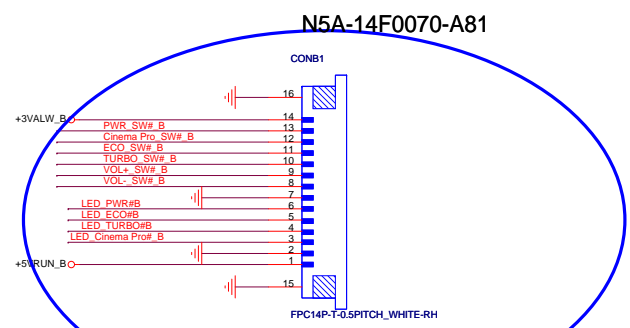
2010/02/01 Reserve for EMI



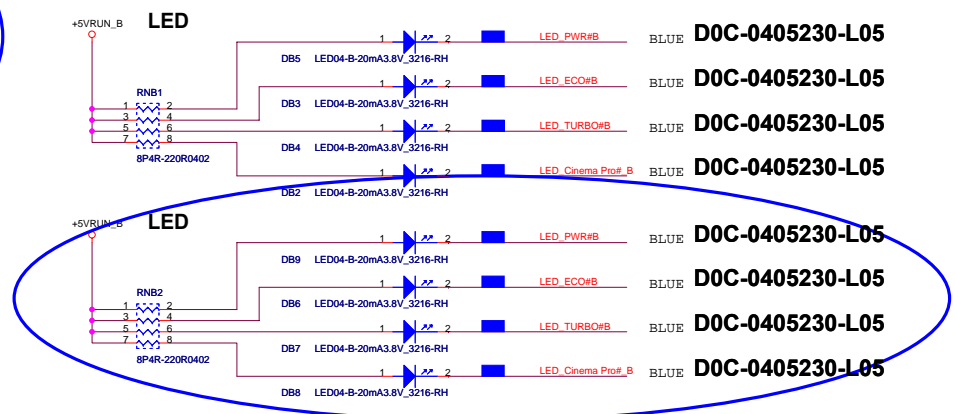
P30-1481B0A-H73, 離手博德(薩摩亞),
P30-1481B0A-D05, 昆頓(定額大陸)



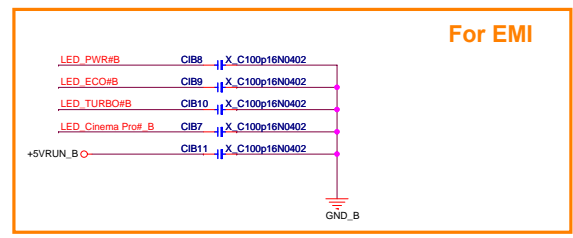
2010/01/25 Add Location holes for ME



2010/01/18 Change pin define to 14 pin



2010/01/22 Add LED for ID request



MSI		MICRO-STAR INT'L CO.,LTD.	
File		Launch Board	
Size	Document Number	Rev	
Custom	MS-1481	0A	
Date:	Wednesday, February 10, 2010	Sheet	46 of 56



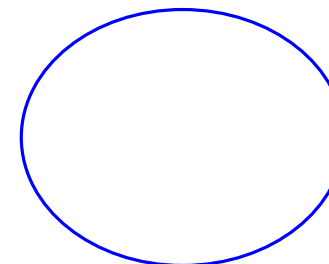
2010/01/26 Add resistor to pull high



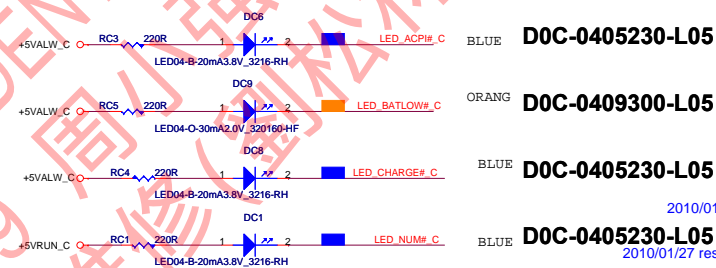
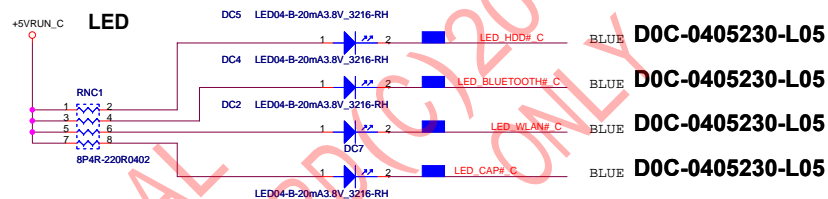
For S8048D-3200 multi finger pin define



2010/01/15 Change pin define to 16 pin



2010/01/05 remove HDD signal MOSFET

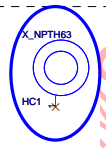
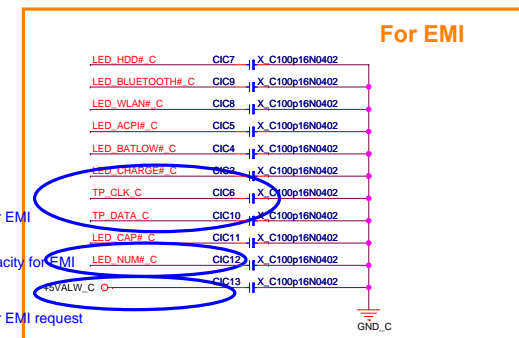


2010/01/26 reserve for EMI

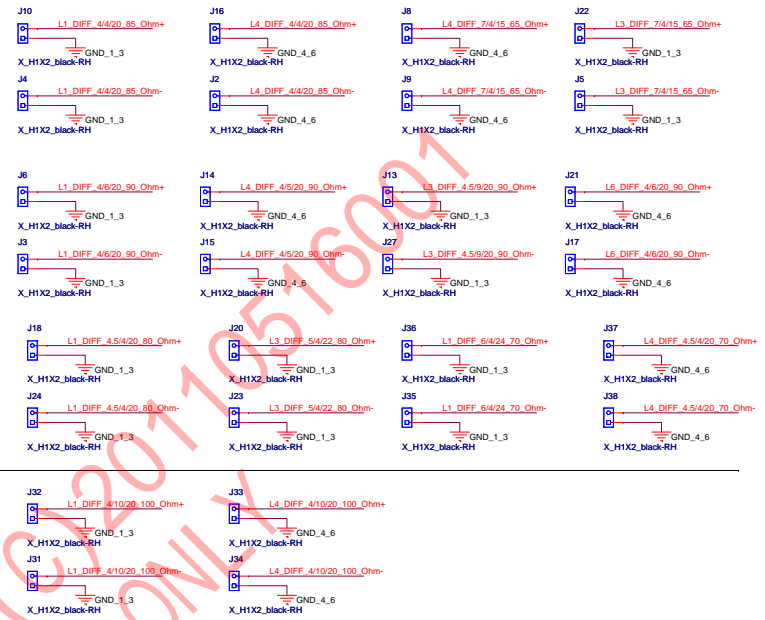
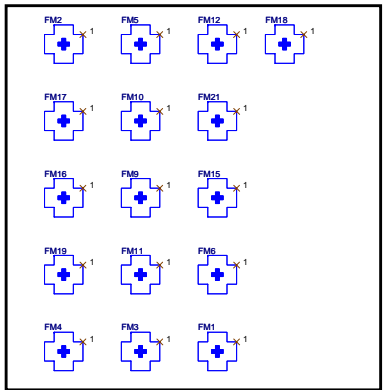
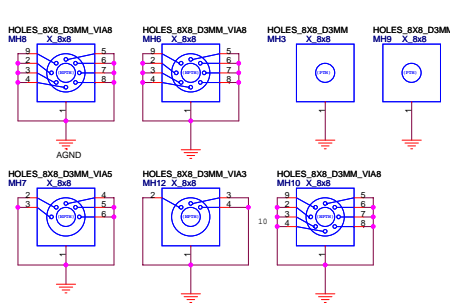
05230-L05

2010/01/27 reserve LED capacity for EMI

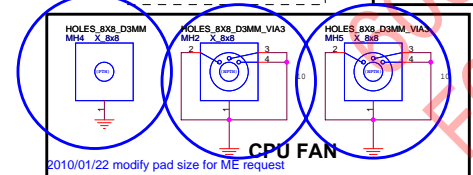
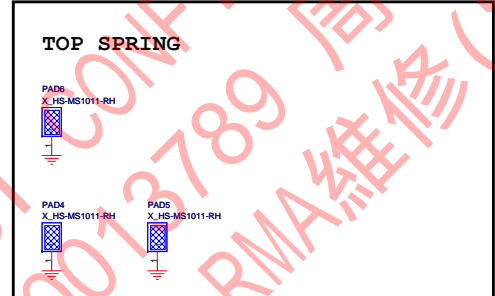
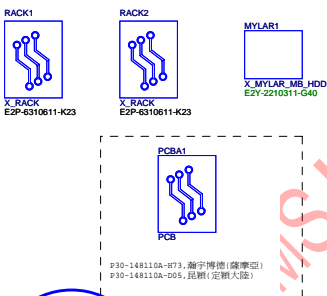
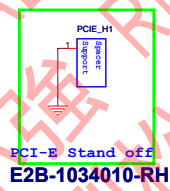
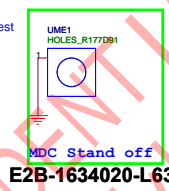
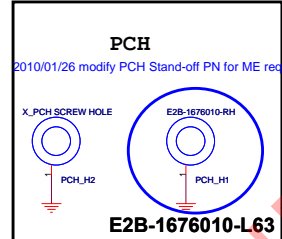
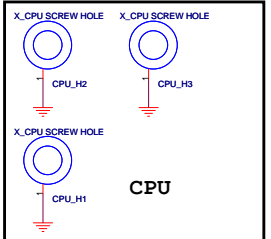
2010/02/01 reserve for EMI request



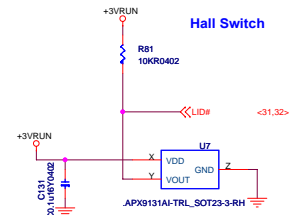
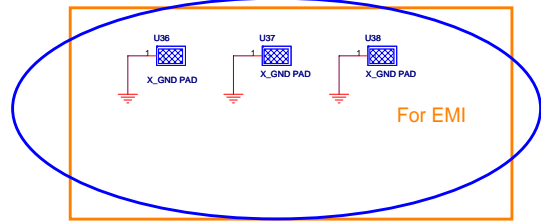
2010/01/25 Add location holes for ME

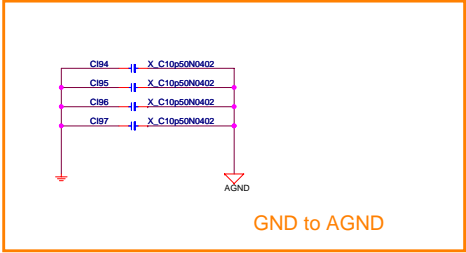
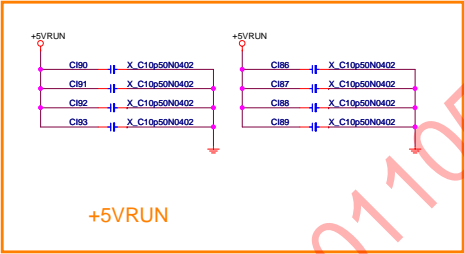
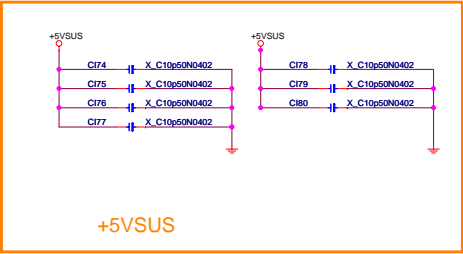
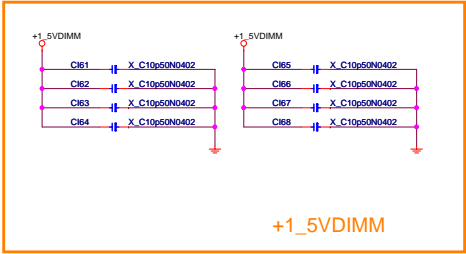
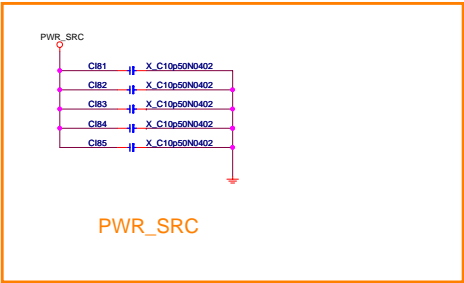
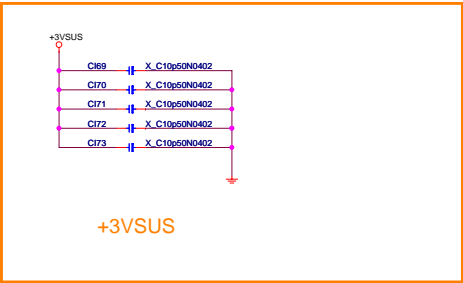
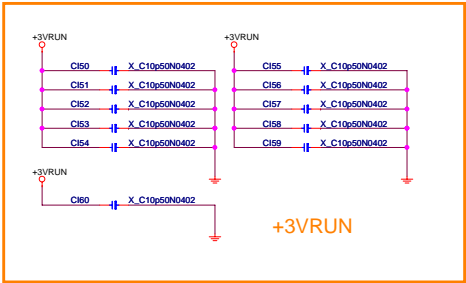


2010/01/19 Change CPU+PCH Screw to holes_r276d185s



2010/01/22 modify pad size for ME request
2010/01/28 modify screw for EMI request

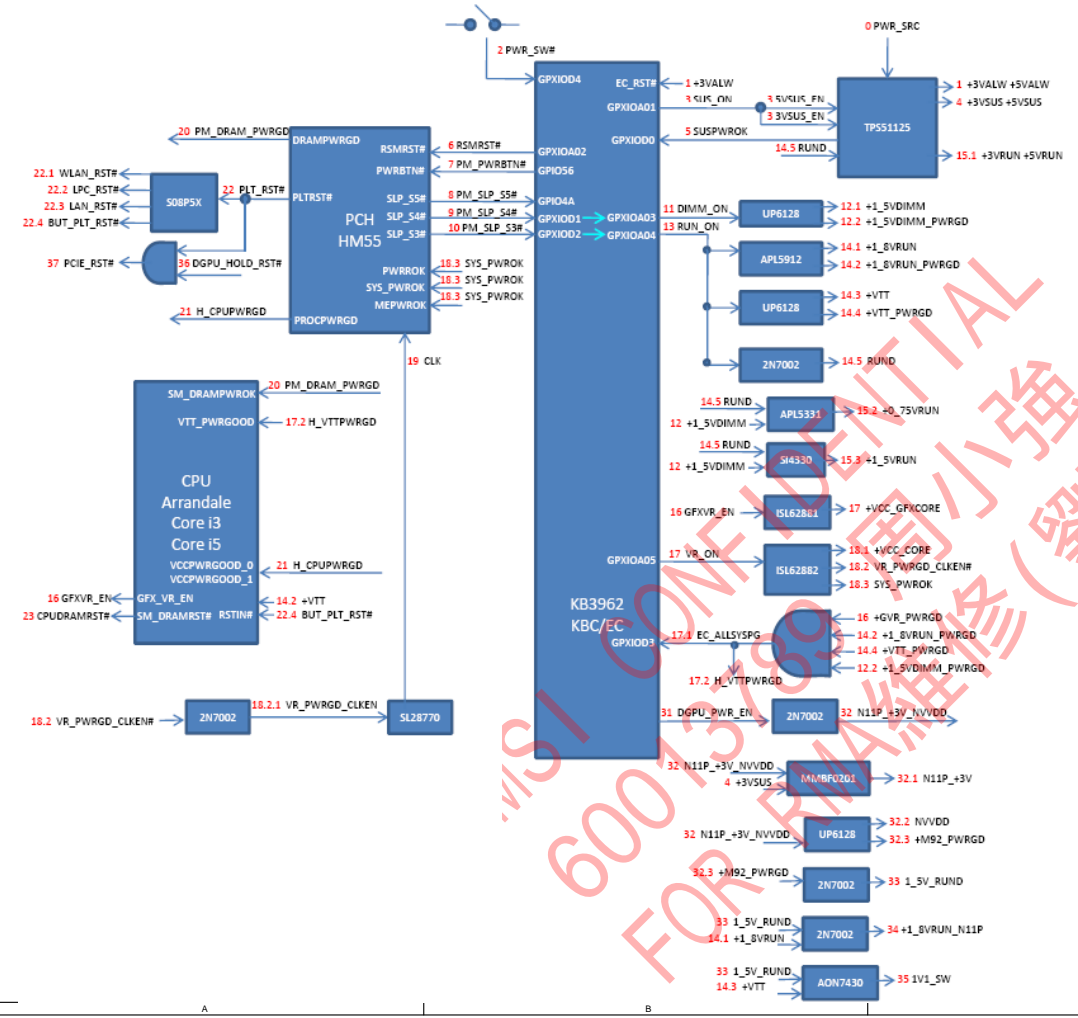




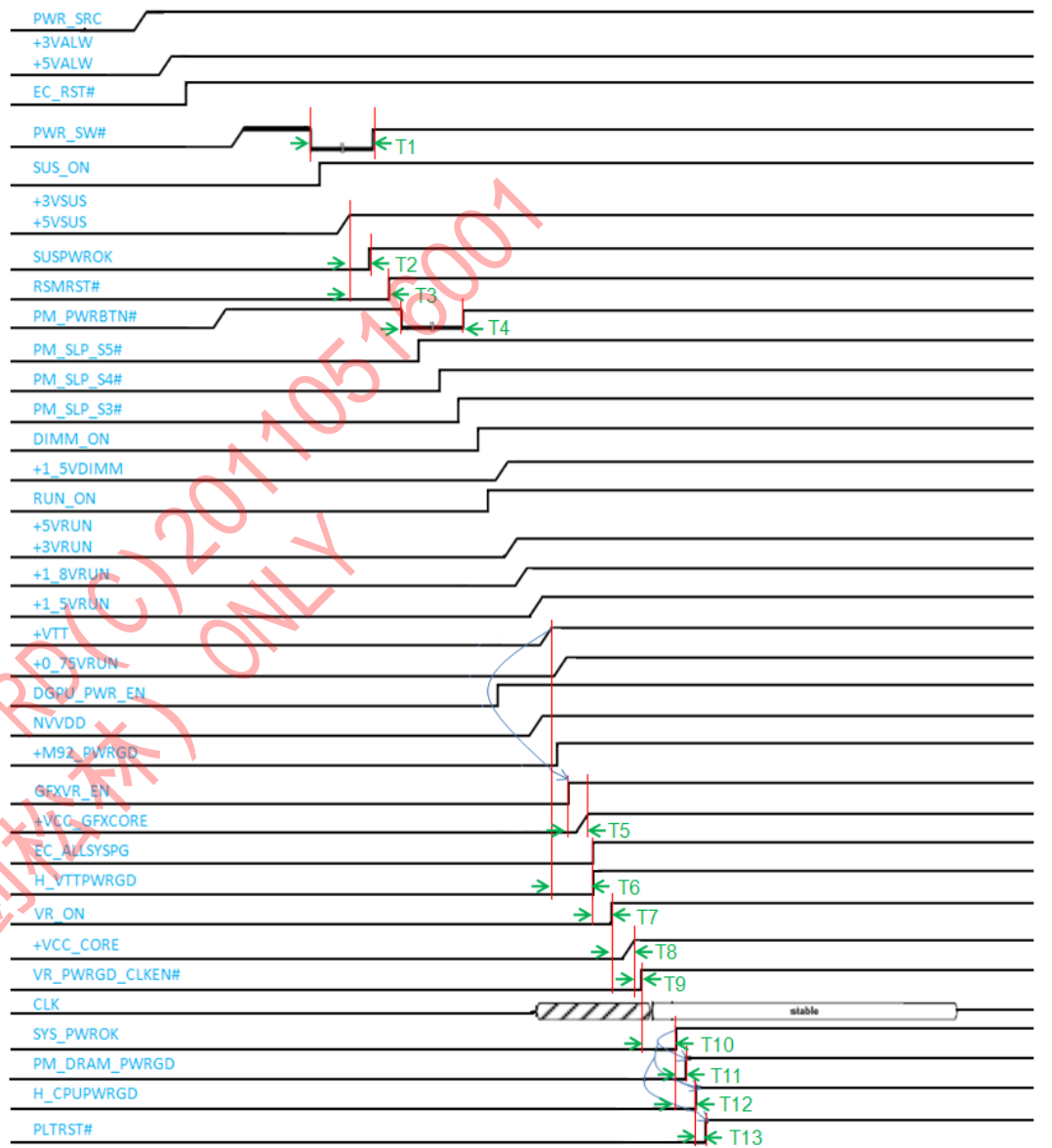
2010/02/01 Reserve power by pass capacity for EMI request

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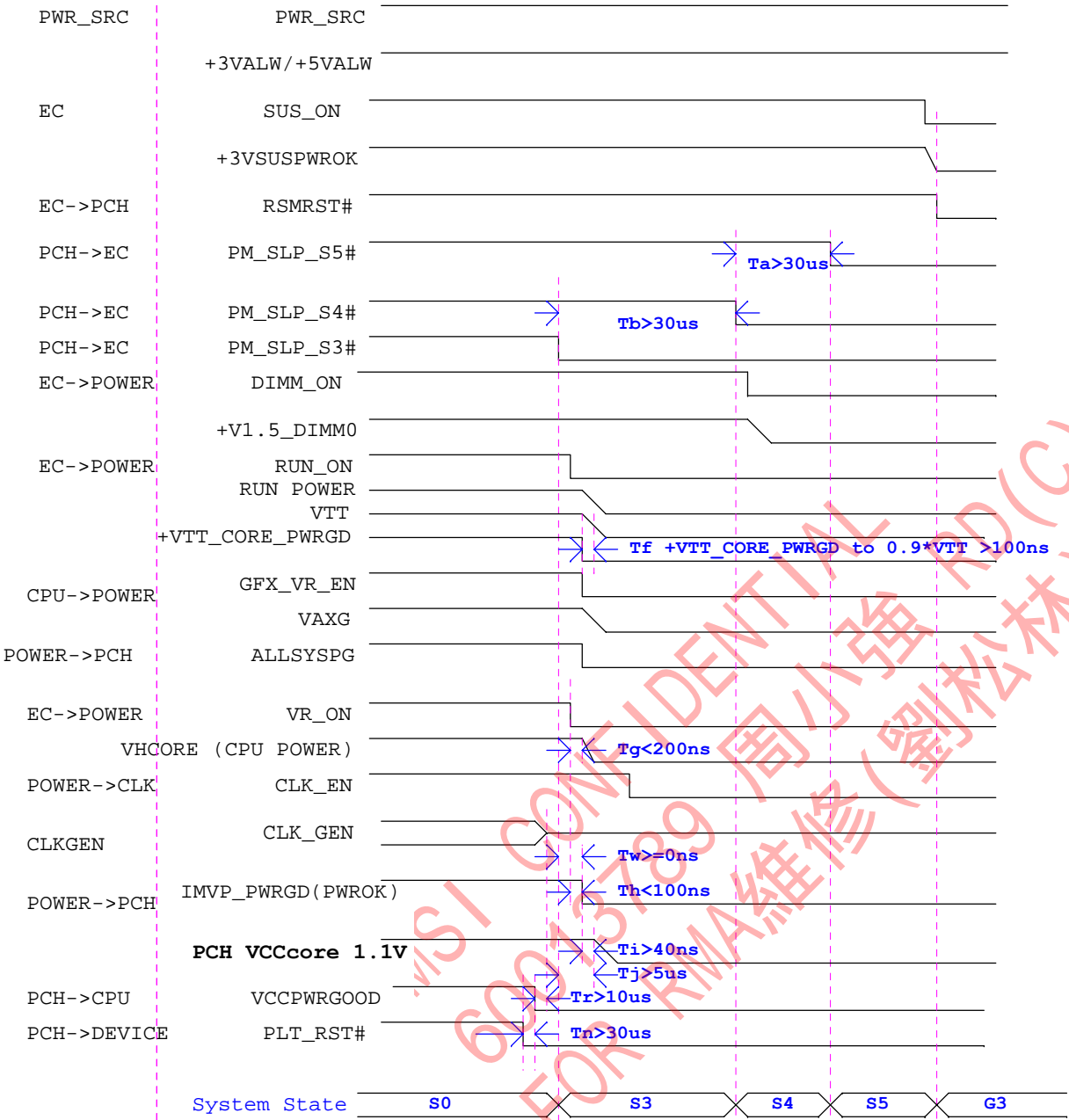
Label	Min	Max	Units	Description
T1	150		ms	
T2	2	2.5	ms	The powergood function is activated with 2 ms internal delay after SUSPWROK goes high. If the output voltage becomes within +/-5% of the target value, PGOOD goes high around 2.5 ms after SUSPWROK goes high.
T3	10		ms	Vcc_SUS stable to RSMRST# deassertion.
T4	150		ms	
T5		1	us	CPU will drive Gfx_VR_EN when VTT ramps. Gfx_VR_EN to Gfx_VID stable. Timing set by Processor.
T6		500	ms	VTT stable to VITTPWRGOOD assertion to the processor.
T7	99		ms	ALL_SYS_PWRGD assertion to IMVP_VR_EN. This timing is generated by EC.
T8		3	ms	
T9	10	100	us	
T10	3	20	ms	IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
T11	1		ms	SYS_PWROK/PCH_PWROK assertion to DRAMPWROK assertion. Timing set by PCH.
T12	1		ms	SYS_PWROK/PCH_PWROK assertion to VCCPWROK/GOOD assertion. Timing set by PCH.
T13	1		ms	VCCPWROK/GOOD assertion to PLTRST# deassertion.



Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3



0A NOTE

- 2009/12/25
- 1.Change Aduio codec form ALC 888 to ALC 269
 - 2.Change LAN Chip from RTL 8111DL to RTL 8111EL
- 2009/12/29
- 1.For Power team request change the power page(P.38~P.43) to same the 16G1
 - 2. Page 21 For Layout request reversal the PCH Azialia arry resistor sequency
 - 3. Page 22 For Layout request reversal the PCH SMBus arry resistor sequency
 - 4. Page 5 Remove PROCHOT# line, Add test point
 - 5. Page 45 ADD VOL+_SW,VOL+_SW,EC0_SW,HIQ_SW,TURBO_SW
- 2009/12/30
- 1.For Card reader ENE suggestion add 4.7K ohm pull hi to 3V
 - 2. P40,P41,P43 delete Nvidia Venthura power desgin

- 2009/12/31
- 1. Page 38 Change power connector
- 2010/01/03
- 1. Page 46 Add TP board
 - 2. Page 12, 13 modify off page symbol
 - 3. Page 35 follow reference schematic remover 3 capacity

- 2010/01/04
- 1. Page 35 follow reference schematic add 10K pull low
 - 2. Page 44 Remove NV I/O 1.8V
 - 3. Page 45 follow ENE suggestion change the capacity to 20P
- 2010/01/05
- 1. Page 3 Change decoupling capacity from X5R to X7R
 - 2. Page 31 Add CRT HSYNC &VSYN level shift
 - 3. Page 47 remove HDD LED MOSFET

- 2010/01/07
- 1. Page 38 For EMI request change capacity from 22p to 10p

- 2010/01/08
- 1. Page 43 For OC reserve adjust voltage schemaitc
 - 2. Page 44 For OC reserve adjust voltage schemaitc

- 2010/01/12
- 1.Page 38 follow Realtek suggestion modify PD# schematic
 - 2.Page 39 Remove power schematic for power team request
 - 3.Page 40 Chagne R1230 from 174K(0603) to 178K(0402) for power team request
 - 4. Page 38 remove OD schematic for Realtek suggestion
 - 5. Page 38 Add and change pull hi resistor to 4.7K
 - 6. Page 38 Change power connector same the 16G1
- 2010/01/13
- 1. Page 32 Change keyboard Connector for 87 Keys
 - 2. Page 33 Change ESATA CONN PN

- 2010/01/14
- 1. Page 47 Change TP Pin define for multi finger
 - 2. Page 42 reserve GFX VID pull & low resistor
 - 3. Page 11 Nvidia Recommend R200 isn't stuff
 - 4. Page 12 Change pull low resistor value form 1% to 5%
 - 5. Page 13 Change pull low resistor value form 1% to 5%
 - 6. Page 18 Change pull low resistor value form 1% to 5%
 - 7. Page 19 Change pull low resistor value form 1% to 5%
 - 8. Page 19 Nvidia recommend change R103 & R104 value from 10K to 2.2K ohm
 - 9. Page 19 Nvidia recommend reserve I2CS for thermal sensor
 - 10. Page 40 For adjust power sequence modify schematic

Begging to now total adding components :81

- 2010/01/15
- 1. Page 9.10 Change reserve capacity value form 2.2uF to 10uF
 - 2. Page 9.10 Remove the x-copper, add verf_ca resistor 10K*2
- 2010/01/18
- 1. Page 19 Add reserve pull hi and pull low resistor for Nvidia recommend
 - 2. Page 32 & 46 Change Connector from 16 pin to 14 pin

- 2010/01/19
- 1. Page 36 Fro EMI request change reserve capacity location
 - 2. Page 39 Fro power team request swap the MOSFET location
 - 3. Page 32 Change the smith trigger unit at schematic
 - 4. Page 43 Change smith trigger part reference
 - 5. Page 34 Reserve Level shift IC pin 38 add 2.2K pull low
 - 6. Page 48 Change CPU+PCH Screw to holes_r276d185s
- 2010/01/20
- 1. Page 33 For Me request change H.D.D connector P/N
 - 2. Page 19 Add GPIO 5 & 6 Pull hi & Pull low resistor for Nvidia request
 - 3. Page 48 Change PCH-Stand-off PN E2B-1431010-L63

- 2010/01/21
- 1. Page 07 Change 0R to X-copper
 - 2. Page 08 Change 0R to X-copper
 - 3. Page 9 Stuff C77 & Stuff Vref CA resister
 - 4. Page 9 Stuff C52 & Stuff Vref CA resister
 - 5. Page 11 Change C155,C256,C272,C196,C268 to no stuff
 - 6. Page 12 Change C413 to no stuff and Add C572
 - 7. Page 18 Change C166,C173,C470 to no stuff
 - 8. Page 21 remove resistor to TP point save for layout space
 - 9. Page 31 Change Pin define and remove reserve component for layout space save and save cost (common used 1471 LVDS cable)
 - 10. Page 24 used LVDS cable same the 1471, can save other LVDS write
 - 11. Page 38 Add capacity for voltage stable
 - 12. Page 33 Remove component to save layout space

- 2010/01/22
- 1. Page 35 Add Q33,R45,C573,U35 for LAN ECO
 - 2. Page 11 Change 0R to x-copper tosave component
 - 3. Page 32 Change array capacity to save layout space
 - 4. Page 46 For ID request Add LED *4
 - 5. Page 41 For power team request modify capacity value from 470uF 10 68uF
 - 6. Page 45 modify screw size for ME
 - 7. Page 23 modify resistor 1K to 10K
 - 8. Page 31 modify R369,R359 to stuff
 - 9. Page 24 remove component to save layout space
 - 10. Page 40 Reserve capacity for fine tune timing
 - 11. Page 30 modify FSA pull high to 10KR
 - 12. Page 30 modify Crystal(Y6) for ME height limit
 - 13. Page 32 Key board follow 1471 pin define

- 2010/01/25
- 1. Page 32 Rechange array capacity to capacity
 - 2. Page 45 Add location holes for ME
 - 3. Page 46 Add location holes for ME
 - 4. Page 47 Add location holes for ME
 - 5. Page 21 BIOS PN pending change to M31-25L3203-M24
 - 6. Page 13 Resistor PN peding change to R11-402AT12-W08
 - 7. Page 19 Resistor PN peding Change to R11-402AT12-W08
 - 8. Page 28 Bead PN pending change to L01-1006084-T19
 - 9. Page 48 For EMI suggestion change MH8 GND to AGND

- 2010/01/26
- 1. Page 48 modify stand-off for ME request
 - 2. Page 12 reserve pull hi resister for Nvidia request
 - 3. Page 13 reserve pull hi resister for Nvidia request
 - 4. Page 47 Add TP CLK & DATA pull hi resistor
 - 4. Page 37 for ME request modify the MDC connectr PN

- 2010/01/27
- 1. Page 48 modify stand-off for ME request
 - 2. Page 25 for layout request swap RN6 pin define
 - 3. Page 37 & 45 connector pin define
 - 4. Page 47 reserve capacity for EMI request

- 2010/01/28
- 1. Page 48 modify screw for EMI request

- 2010/01/29
- 1. Page 34 Add resistor for TI suggestion

- 2010/02/01
- 1. Page 47 Swap TP connector pin define for ME cable
 - 2. Page 45 no stuff USB EMI common choke
 - 3. Page 37 no stuff USB EMI common choke
 - 4. Page 45 Reserve capacity for EMI request
 - 5. Page 47 Reserve capacity for EMI request
 - 6. Page 47 Reserve capacity for EMI request
 - 7. Page 49 Reserve power by pass capacity for EMI request
 - 8. Page 48 Reserve GND Pad for EMI request
 - 9. Page 41 For high frequency issue modify 68uF to 100uF

- 2010/02/02
- 1. Page 41 Change net and add net name for vendor suggestion
 - 2. Page 41 Reserve 330uF capacity for high frequency issue

- 2010/02/03
- 1. Page 37 USB Pin 2 & Pin 3 Pin 2 swap
 - 2. Page 45 Delete USB MEC pin to GND
 - 3. Page 45 Delete USB MEC pin to GND

2010/02/09


Note for 0B CN4,VGA1,CN2,USB1,MICA1,LOUT1 fot 產線製程改爲60階,0B需改回原本階層

2010/02/09

Note 1 CN4,VGA1,CN2,USB1,MICA1,LOUT1 for SMTchange to 60 status,remind 0B version must change to default status

Note 2. remind 0B version msut change 14.318MHz & 25MHz crystal to mainstream source

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Title			
0B NOTE			
Size	Document Number		Rev
Custom	MS-1481		0A
Date:	Wednesday, February 10, 2010		Sheet 54 of 56

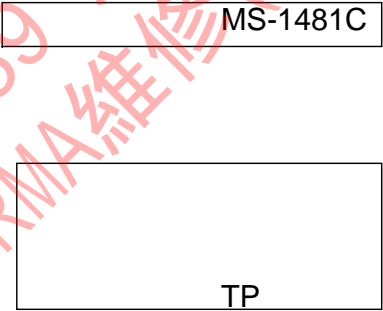
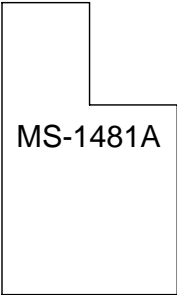
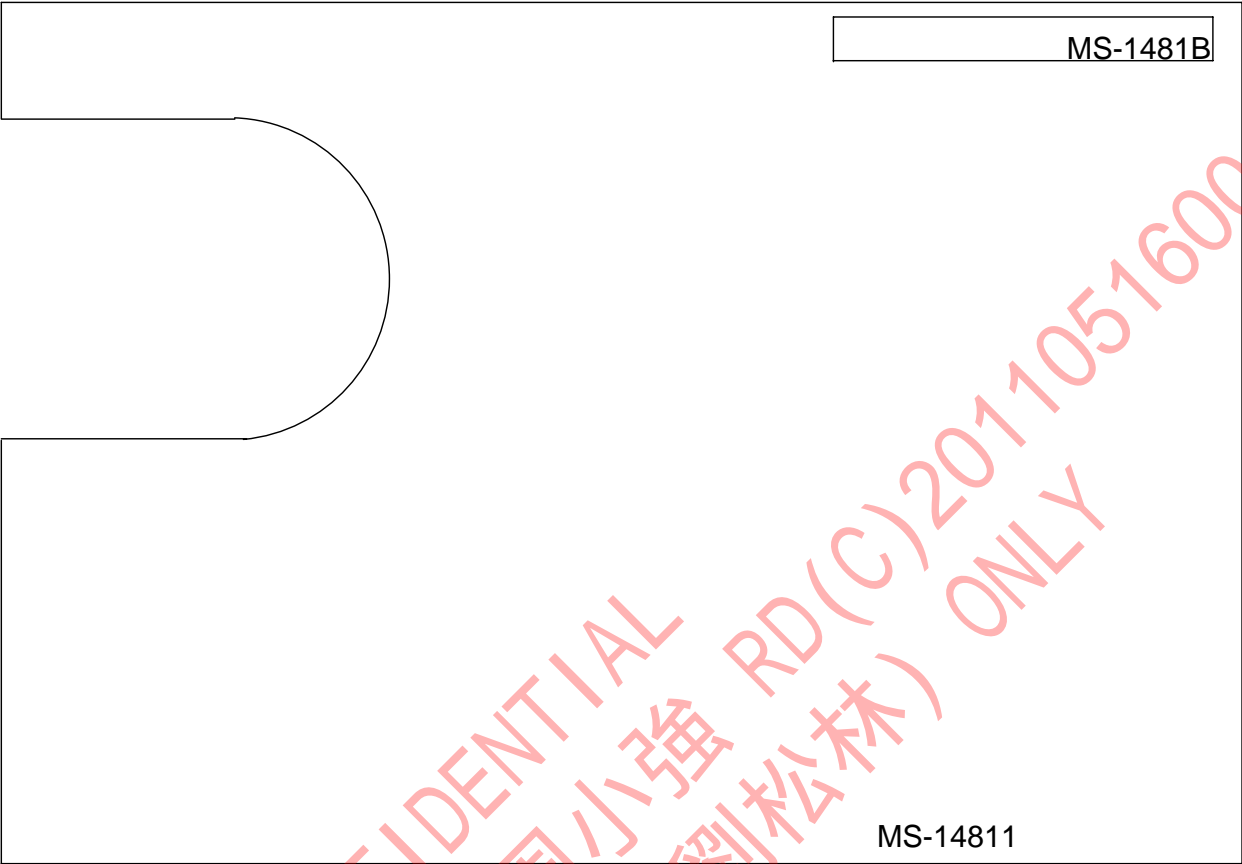
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Title
1.0 NOTE

Size A	Document Number MS-1481	Rev 0A
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Title			
TOPOLOGY			
Size	Document Number		Rev
B	MS-1481		0A
Date:	Wednesday, February 10, 2010	Sheet	56 of 56